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Strained-layer InGaAs and InAlAs structures have been grown by molecular beam epitaxy on lattice-mismatched GaAs substrates in order to examine various material properties which may be utilized advantageously for certain devices. The emphasis has been placed on the development of a heterojunction insulated-gate field effect transistor (HIGFET) using lattice-mismatched InGaAs and InAl As layers to demonstrate the effective utilization and advantages of strained layers.

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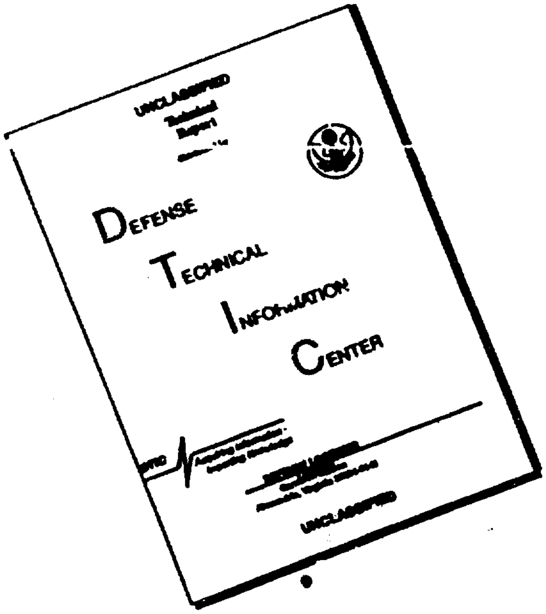
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To increase the fractional In content in the device channel and therefore improve the device characteristics without giving up performance due to defects generated by a large lattice-mismatch with the GaAs substrate, it becomes necessary to interpose a buffer which can act as an artificial substrate for the channel, in essence "decoupling" the channel from the true substrate. This has been accomplished by designing buffer structures which induce lattice constant shifts to values equivalent to unstrained $In_{0.30}Ga_{0.70}As$ or $In_{0.15}Ga_{0.85}As$. In order to protect the channel and subsequently grown layers from propagating dislocations generated at the buffer/substrate interface, a strained layer superlattice (SLS) lattice-matched to the new artificial lattice constant is inserted within the buffer to act as a dislocation filter. The alternating strain field in the SLS acts to bend aside any upward propagating dislocations and force them away from the active region of the device. X-ray diffractometry, transmission electron microscopy, Hall and conductivity measurements, and the final transistor characteristics were used to evaluate the quality of these buffer structures.

The HIGFET uses a heavily doped 150-200Å n-type $In_{0.30}Ga_{0.70}As$ channel layer. This layer is lattice-matched in the case of an $In_{0.30}Ga_{0.70}As$ equivalent buffer and pseudomorphic for the $In_{0.15}Ga_{0.85}As$ equivalent buffer. An undoped and depleted InAlAs layer is situated over the channel layer beneath the gate metallization and acts as a quasi-insulator producing a metal-insulator-semiconductor gate-type geometry. The InAlAs layer is grown lattice-matched to the buffer lattice constant to prevent further generation of dislocations and has an indirect bandgap at these compositions. As a result, a large direct to indirect conduction band discontinuity exists between the channel and quasi-insulator and may be taken advantage of. HIGFETs have been fabricated with an extrinsic transconductance of $g_m = 140mS/mm$ obtained for 2 μm gate lengths.

Two doctoral dissertations were written and accepted as satisfaction, in part of the Ph.D degree in Applied Physics:

(1) UNIVERSITY OF CALIFORNIA, SAN DIEGO

InGaAs/InAlAs Lattice-Mismatched
Heterojunction Insulated-Gate Field Effect Transistors Grown on GaAs

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical Engineering (Applied Physics)

by

Peter Chu

1990

(2) UNIVERSITY OF CALIFORNIA, SAN DIEGO

Anisotype Heterojunction Field-Effect Transistors
for Digital Logic Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical Engineering (Applied Physics)

by

Chi-lieh Lin

1991

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REFERENCE: N00014-89-J-2023;
Dr. H. Wieder, Principal Investigator

Dear John

In accordance with Attachment Number 2 of the above referenced grant, enclosed is one copy of the final technical report.

Sincerely

Lynelle A. Gehrke

Lynelle A. Gehrke
Administrative Analyst

Enclosure: 1

cc: Howard Lessoff, NRL, Code 6820 (3)
Director, NRL, Code 2627 (1)
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List of publications in the Archival Literature on work partially supported by this Contract:

1. C. L. Lin, H. H. Wieder, *J. Vac. Sci. Technol.* **A9**(3), 858 (1991), "Low-Temperature Processing and Characterization of Metastable, Anisotype Heterojunction Gate, Strained-Layer Field-Effect Transistors".
2. J. Shin, K. M. Geib, C. W. Wilmsen, P. Chu and H. H. Wieder, *J. Vac. Sci, Technol* **A9**, 1029 (1991). "The thermal oxidation of Al-GaAs".
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4. P. Z. Lee, C. L. Lin, J. C. Ho, L. G. Meiners and H. H. Wieder, *J. Appl. Phys.* **57**(9), 4377 (1990). "Conduction band discontinuities of $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ n-isotype heterojunctions"
5. C. L. Lin, J. M. Fernández, H. H. Wieder, *IEEE Electron Device Letters.* **11**(1) 30 (1990). "An Anisotype $GaAs/In_xGa_{1-x}As$ Heterojunction Field-Effect Transistor for Digital Logic Applications",

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InGaAs/InAlAs Lattice-Mismatched Heterojunction Insulated-Gate Field Effect Transistors Grown on GaAs

Abstract

Strained -layer InGaAs and InAlAs structures have been grown by molecular beam epitaxy on lattice-mismatched GaAs substrates in order to examine various material properties which may be utilized advantageously for certain devices. The emphasis has been placed on the development of a heterojunction insulated-gate field effect transistor (HIGFET) using lattice-mismatched InGaAs and InAl As layers to demonstrate the effective utilization and advantages of strained layers.

To increase the fractional In content in the device channel and therefore improve the device characteristics without giving up performance due to defects generated by a large lattice-mismatch with the GaAs substrate, it becomes necessary to interpose a buffer which can act as an artificial substrate for the channel, in essence "decoupling" the channel from the true substrate. This has been accomplished by designing buffer structures which induce lattice constant shifts to values equivalent to unstrained $In_{0.30}Ga_{0.70}As$ or $In_{0.15}Ga_{0.85}As$. In order to protect the channel and subsequently grown layers from propagating dislocations generated at the buffer/substrate interface, a strained layer superlattice (SLS) lattice-matched to the new artificial lattice constant is inserted within the buffer to act as a dislocation filter. The

alternating strain field in the SLS acts to bend aside any upward propagating dislocations and force them away from the active region of the device. X-ray diffractometry, transmission electron microscopy, Hall and conductivity measurements, and the final transistor characteristics were used to evaluate the quality of these buffer structures.

The HIGFET uses a heavily doped 150-200Å n-type $In_{0.30}Ga_{0.70}As$ channel layer. This layer is lattice-matched in the case of an $In_{0.30}Ga_{0.70}As$ equivalent buffer and pseudomorphic for the $In_{0.15}Ga_{0.85}As$ equivalent buffer. An undoped and depleted InAlAs layer is situated over the channel layer beneath the gate metallization and acts as a quasi-insulator producing a metal-insulator-semiconductor gate-type geometry. The InAlAs layer is grown lattice-matched to the buffer lattice constant to prevent further generation of dislocations and has an indirect bandgap at these compositions. As a result, a large direct to indirect conduction band discontinuity exists between the channel and quasi-insulator and may be taken advantage of. HIGFETs have been fabricated with an extrinsic transconductance of g_m=140mS/mm obtained for 2μm gate lengths.

Heterojunctions

The growth of two different semiconductors adjacent to one another leads to the formation of a heterojunction in which the alignment of energy bands results in unique properties. Because two materials adjacent to one another may have different bandgaps, there will exist a bandedge discontinuity at the interface. Furthermore, differences in their dielectric constant or index of refraction result, likewise, in discontinuities in these parameters. Of principal interest here, will be how the bandedge discontinuity is formed.

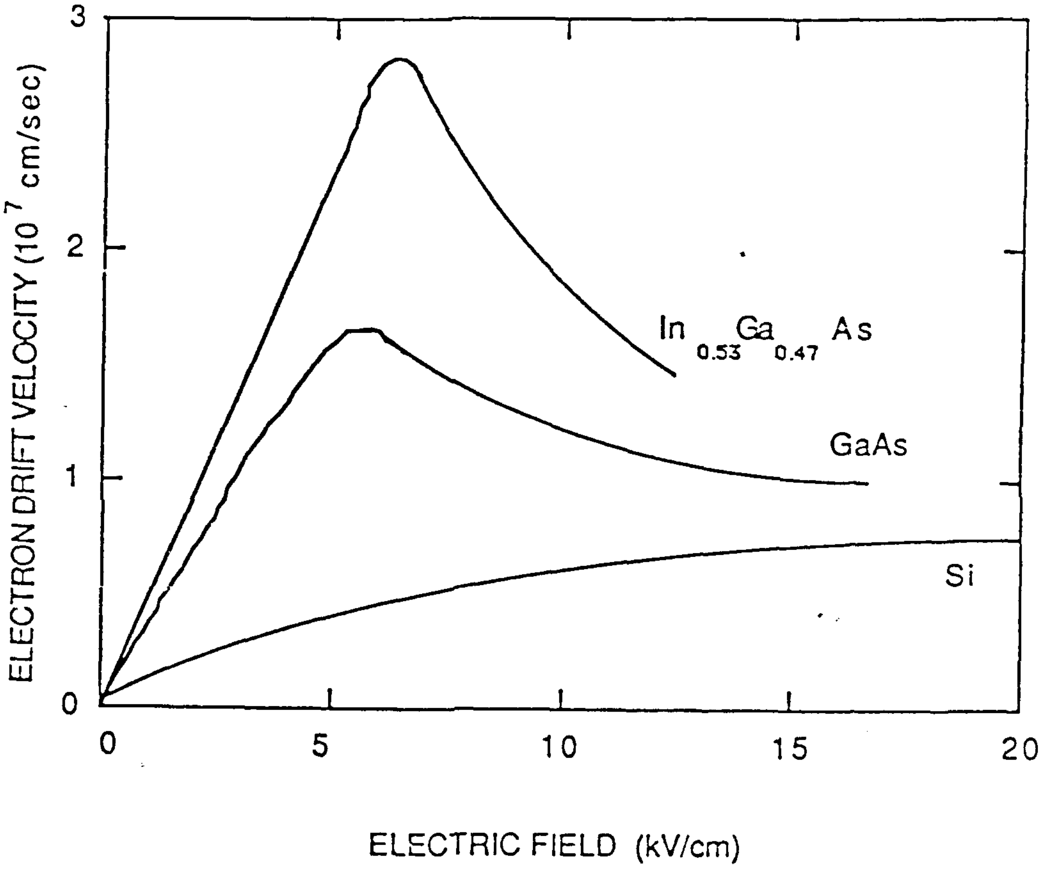
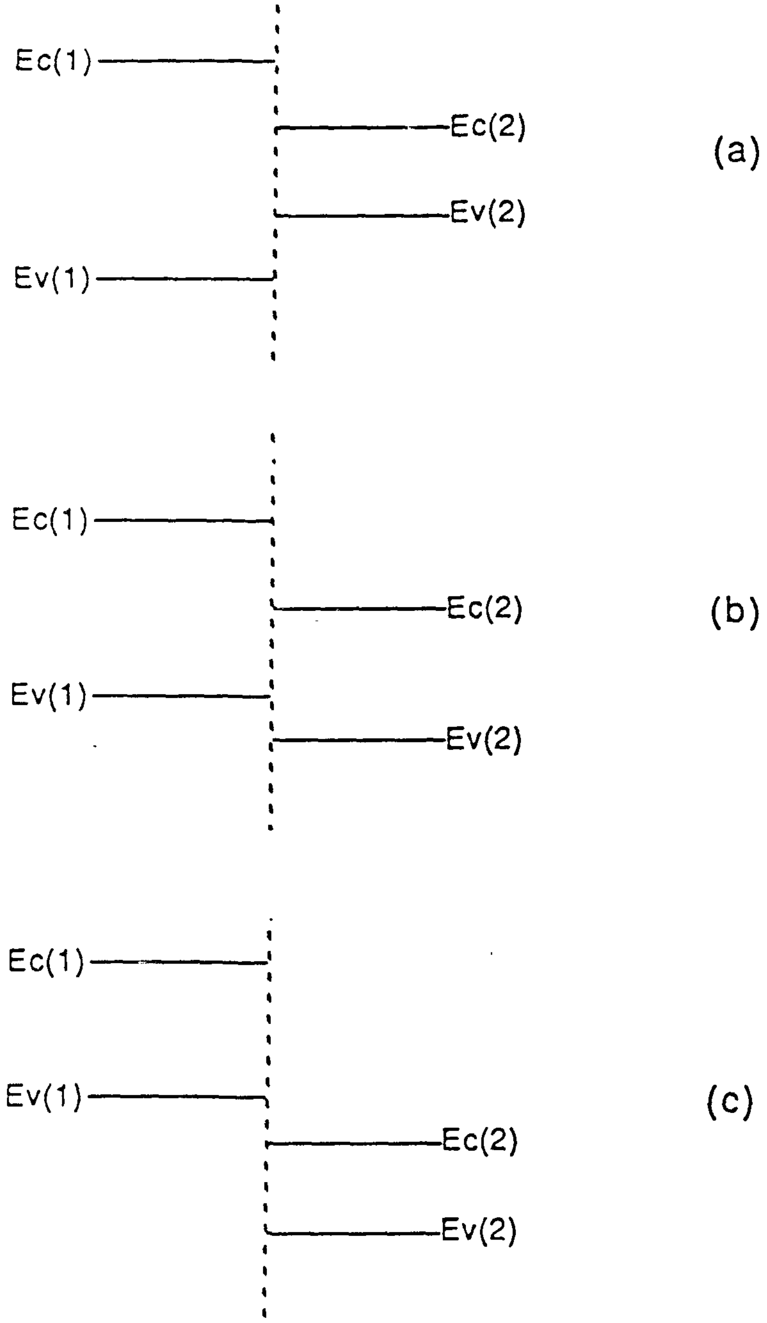


Figure 1.8: A comparison of the room temperature electron drift velocity with electric field for three uniformly bulk-doped semiconductors of $n=10^{15}$ cm^{-3}.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(c)

Figure 1.9: The possible bandgap alignments: (a) straddling lineup; (b) staggered lineup; and (c) broken gap lineup.

Figure 1.9 shows three possible equilibrium band diagrams which may occur when a heterojunction is created. Fortunately, the straddle-type bandgap alignment is dominant in the material systems considered here. This type of alignment is typically characterized by a depletion of electrons from the large bandgap material and an accumulation in the small bandgap material. This is the result of the balance of charge induced when the Fermi-levels in both materials are aligned at equilibrium. Of principal interest when considering bandedge discontinuities is the barrier formed in the conduction band at the heterojunction. It may be used to confine electrons and limit the injection of electrons across it.

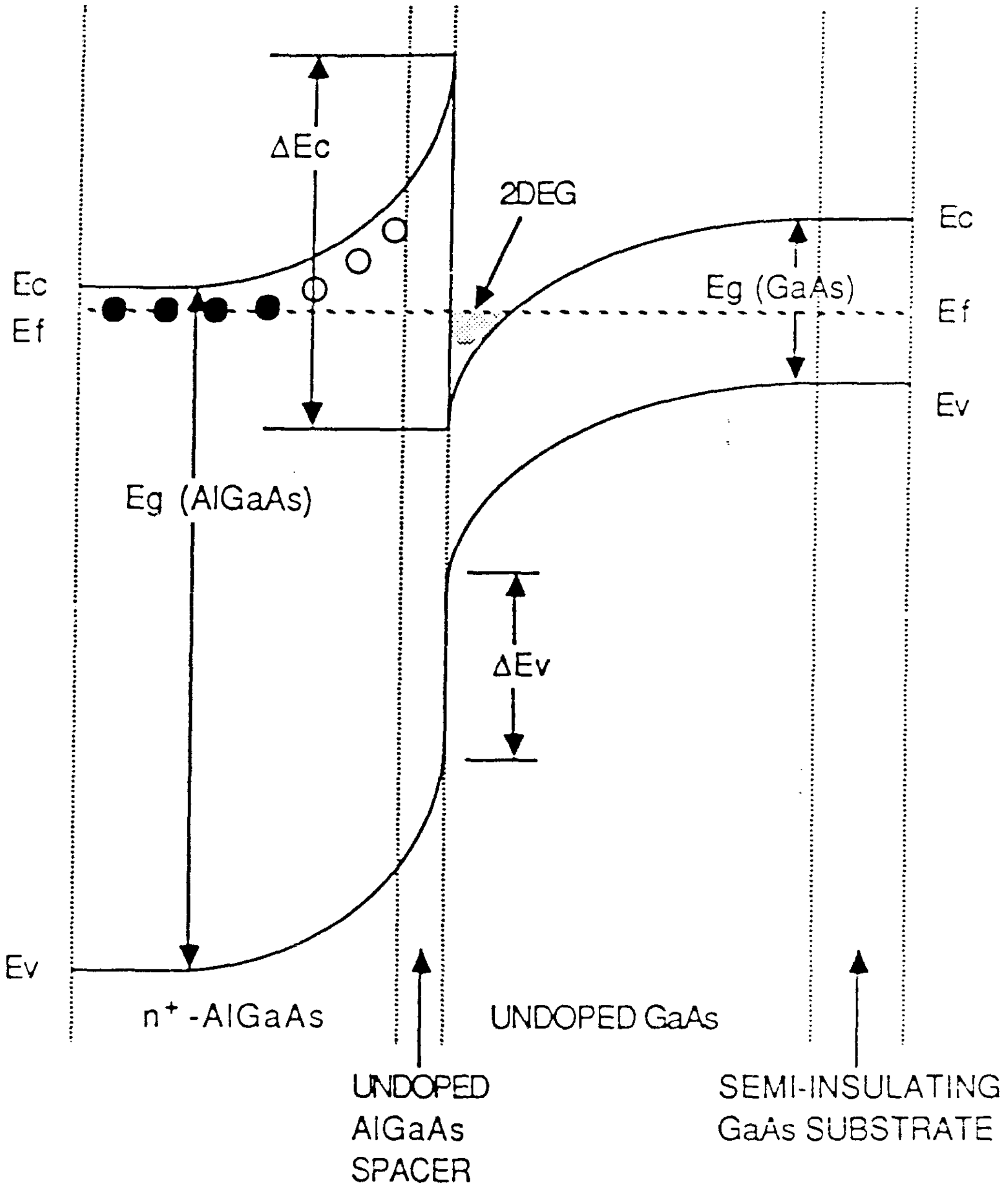
The determination of the bandedge discontinuities continues to be a topic of ongoing debate. While no theoretical argument has completely explained a method for determining the discontinuity, enough experimental data[8] has been accumulated to hazard a prediction of the bandedge discontinuity. In order to simplify the consideration of different material combinations, the empirical relationship

$$\Delta E_c = 0.60\,\Delta E_g\,, \tag{1.1}$$

where ΔE_c is the conduction band discontinuity and ΔE_g is the total difference in bandgaps, will be used.

III-V Heterojunctions

The lattice-matched GaAs/$Al_{0.30}Ga_{0.70}As$ heterostructure system grown on GaAs and the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure system grown on InP are among the most widely studied. The double heterojunction GaAs/$Al_xGa_{1-x}As$ laser was first demonstrated successfully in 1971, and promoted interest in both photonic devices as well as electronic devices utilizing these materials. In the push for higher speed devices, better intrinsic electrical properties, such as mobility, were demanded of materials. The current center of attention on the $In_xGa_{1-x}As/In_xAl_{1-x}As$ system compared to that of the $GaAs/Al_xGa_{1-x}As$ system is related to the improved mobility and lower effective mass of electrons in an $In_xGa_{1-x}As$ channel compared to those in a GaAs channel. Key to the development of heterostructure FETs is the utilization of a two-dimensional electron gas (2DEG) which, under proper conditions, may form at the interface of a heterojunction. The presence of an accumulation layer or inversion layer at the heterointerface was predicted long ago, and through the selective doping of the heterostructure, realization of a 2DEG at the interface is possible. The formation of this 2DEG localized in a quantum well at the heterointerface on the small bandgap material side is caused by the depletion of electrons from the highly doped large bandgap material and an accumulation of those carriers in the narrow bandgap material. The electrons are basically transferred due to the heterojunction. This "modulation" doping results in the spatial separation of ionized impurities and free carriers. Furthermore, since carriers and ionized impurities remain spatially separated by the heterojunction, Coulomb electron-donor scattering is reduced and carrier mobility enhanced. Figure 1.10 shows an energy band diagram of an n^+-AlGaAs/GaAs heterojunction in which a 2DEG is formed. Such 2DEG layers have been verified by observing the Shubnikov-de Haas oscillations of the conducting electrons and determining their dependence with respect to the angle between the applied magnetic fields and the direction normal to the interface. Modulation doping may be applied in certain configured FETs, which will be discussed next.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n⁺ -AlGaAs
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UNDOPED
AlGaAs
SPACER
SEMI-INSULATING
GaAs SUBSTRATE

Figure 1.10: Energy bandgap diagram of an n$^+$-AlGaAs/GaAs heterojunction.

III-V Heterostructure FETs

The Modulation-doped FET

Modulation doped field effect transistors (MODFET) are also called high electron mobility transistors (HEMT), two-dimensional electron gas field effect transistors (TEGFET), or selectively doped heterostructure field effect transistors (SDHFET). They continue to be record breaking devices for high frequency, high speed operations. Advanced device designs use superlattices, delta-doping schemes,[9] and inverted structures[10] to enhance device characteristics. A cross-section of the MODFET is shown in Fig. 1.11. This structure relies on the modulation doping of the GaAs by a heavily doped AlGaAs layer in near proximity to the channel. Adjacent to the channel is an undoped AlGaAs layer which acts as a spacer. The spacer thickness is optimized to prevent accidental real-space transfer of hot carriers back from the channel to the n^+-AlGaAs layer. Furthermore, it enhances the spatial separation of the ionized impurities from the conducting channel layer so as to reduce Coulombic scattering. Lastly, it prevents any accidental diffusion of dopant atoms during growth and processing from entering the channel layer. A 2DEG is formed at the interface in the GaAs due to the modulation doping, and conduction takes place here. The gate electrode is deposited following a recessed etch. The depth of the recess etch is chosen such that the surface depletion of the semiconductor is equivalent to a depth where the n^+-AlGaAs layer is fully depleted. The importance here is to assure perfect modulation efficiency. Over etching would mean fewer carriers in the channel immediately beneath the gate. Under etching could mean the presence of secondary charges, due to the incomplete transfer of charges from the doped layer to the channel. Secondary charges

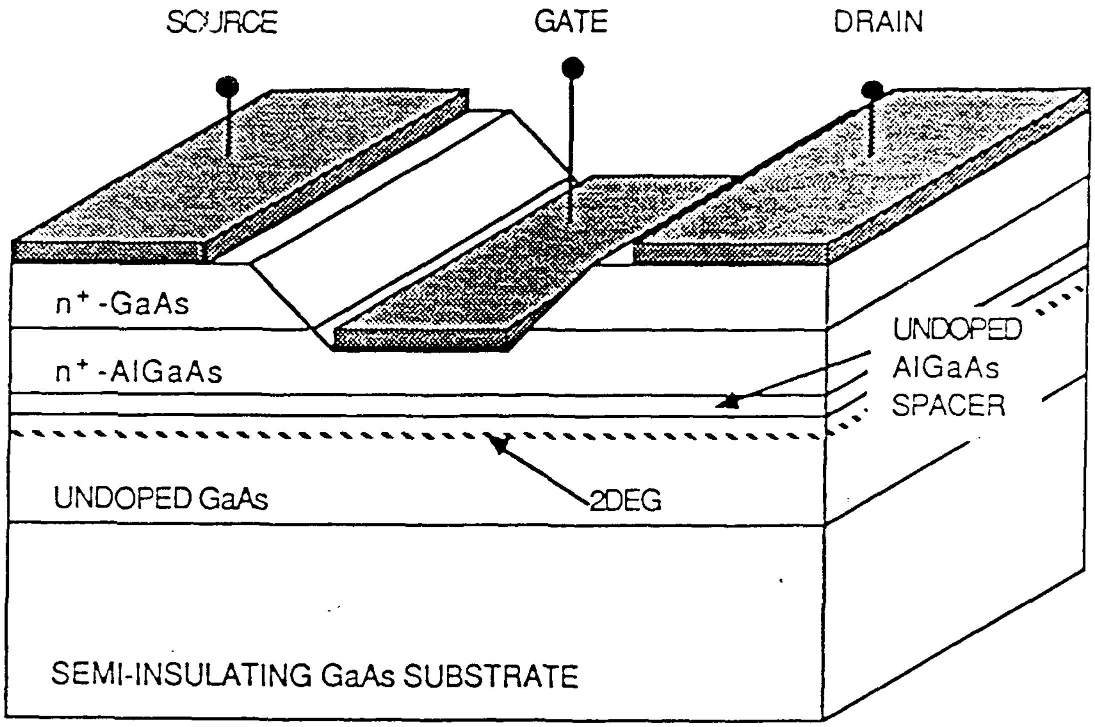
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Figure 1.11: Cross-sectional view of an AlGaAs/GaAs MODFET.

under the gate electrode which would degrade the modulation efficiency of the gate and reduce the gate resistance to leakage. Furthermore, carriers in the n^+-AlGaAs layer represent a potential parasitic conduction path in parallel with the channel. The recess etch is an important processing step since it will affect the threshold voltage. In general, operation of the device is dependent on the polarity and magnitude of the voltage applied to the gate which will effect the electron density in the 2DEG. The upper surface of the device includes a heavily doped n^+-GaAs which facilitates the formation of ohmic contacts for the source and drain electrodes.

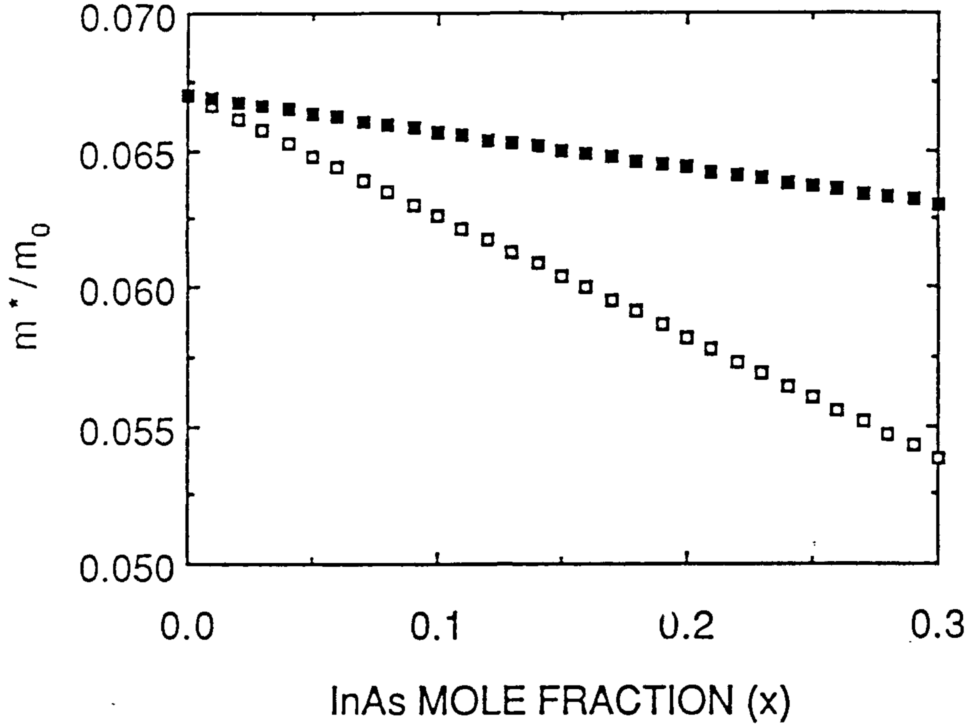


Figure 1.12: Effect of strain on electron effective mass for $In_xGa_{1-x}As$ grown on GaAs. Open squares show the unstrained electron effective mass for varying compositions of InGaAs. Closed squares show the strained electron effective mass for varying compositions of InGaAs.

Modulation doping is in no way restricted to lattice-matched material systems. Current research has emphasized the advantages of using strained materials.[11,12] Of particular interest is the $Al_xGa_{1-x}As/In_xGa_{1-x}As/GaAs$ system and the strained $In_xGa_{1-x}As/In_xAl_{1-x}As/InP$ system. These "pseudomorphic" MODFETs are an improvement over the $GaAs/Al_{0.30}Ga_{0.70}As$ system since the increase in InAs molar fraction of the channel layer results in superior electron mobility, electron velocities, and lower electron

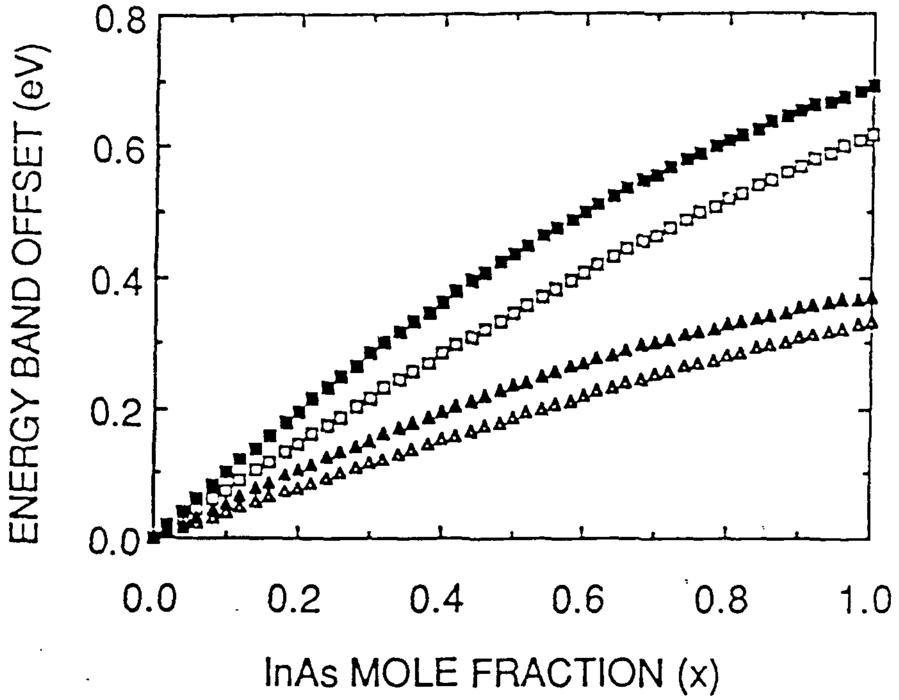


Figure 1.13: Effect of strain on the bandedge discontinuities for $In_xGa_{1-x}As$ grown on GaAs. The closed squares show ΔE_C for unstrained (relaxed) InGaAs on GaAs. The open squares show ΔE_C when the InGaAs layer is strained (pseudomorphic) with respect to its GaAs substrate. The closed triangles show ΔE_V for unstrained (relaxed) InGaAs on GaAs. The open triangles show ΔE_V when the InGaAs layer is strained (pseudomorphic) with respect to its GaAs substrate.

effective masses compared to GaAs channels. However, material improvements are limited by the extent in which high quality $In_xGa_{1-x}As$ may be grown on GaAs substrates. As the channel's InAs content is increased, the lattice constant of the material increases as well. Excessive strain resulting from too much In will result in the formation of defects detrimental to device operation. Furthermore the advantages of strained material cannot be assessed by simple examination of the unstrained properties of that material. Improvements made by changing the compositions are lessened if the layers remain strained. This can be seen in Fig. 1.12 where the effect of strain is visible on the electron effective mass. The plot uses the equations of Liu *et al.*[13] Strain-induced bandgap shifts in the material may also be observed. These strain-induced shifts in the energy bandgap structure of the material will in turn influence the bandgap discontinuities formed at any heterointerfaces. An example is shown in Fig. 1.13 for strained $In_xGa_{1-x}As$ deposited on unstrained GaAs substrates. The plot illustrates calculations using the assumptions of Eq. 1.1 and equations outlined by Dahl.[14]

The Heterojunction Insulated-Gate Field Effect Transistor

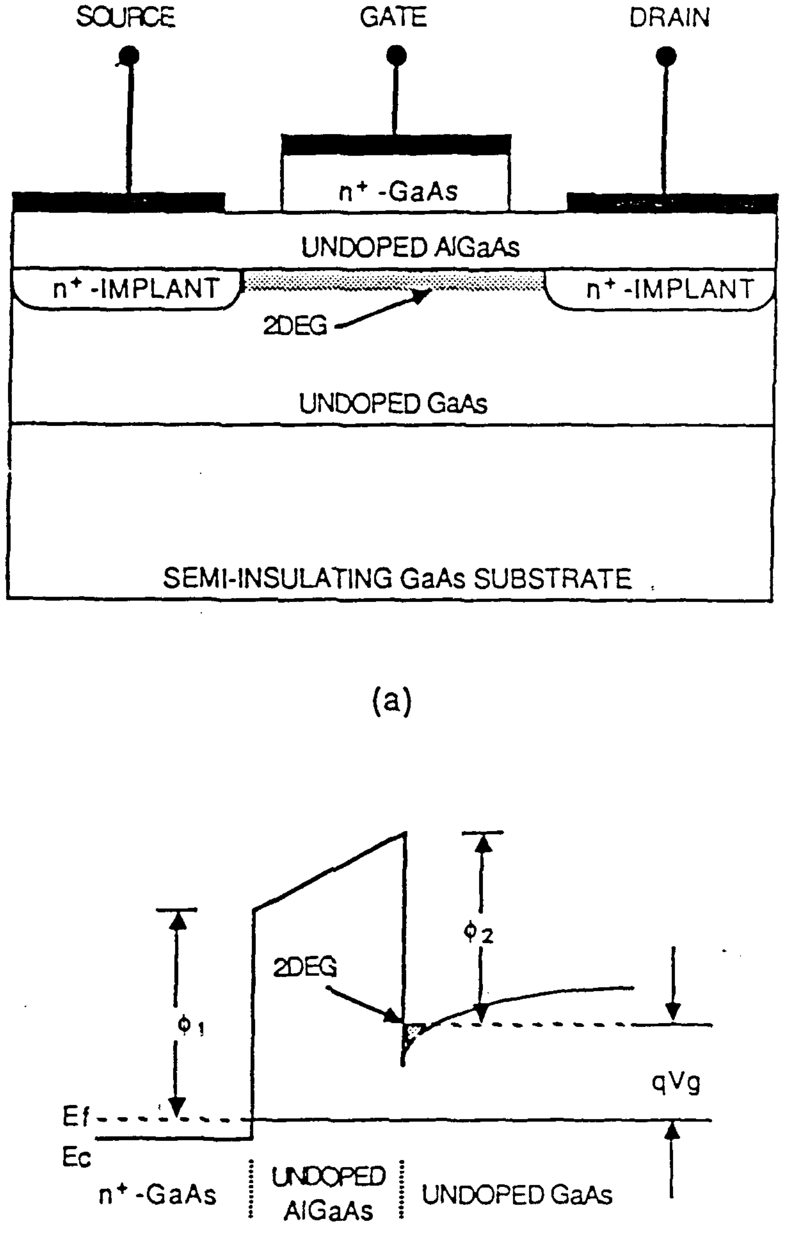
The heterojunction insulated-gate field effect transistor (HIGFET)[15,16,17] is an attempt to create an MIS-like device with characteristics similar to those in current silicon-MOS technology, which has enjoyed great success. The difference in the HIGFET, however, is the application of a semiconductor quasi-insulator which replaces the conventional dielectric or oxide type insulator. In general, III-V materials lack high quality insulators; most have problems associated with active interface states at the insulating layer/semiconductor interface or bulk states within the insulating layer. Although not all devices have reportedly poor performances,[18] the single step epitaxial growth of the HIGFET compared to the typical two-step process for MISFETs utilizing conventional insulators allows one to avoid contamination and passivation problems of the surface. These problems often occur in two step processes where the sample must be transferred between deposition systems. In the HIGFET, the quasi-insulator is composed of a fully depleted, undoped, large bandgap semiconductor layer and it is proposed that the density of interface states within the semiconductor-semiconductor heterojunction is less than that found in conventional MIS structures. Of particular importance is the assumption that the combination of a large bandgap, inducing a large bandedge discontinuity adjacent to the channel layer and thus enhancing confinement, along with surface depletion, which is improved by the undoped nature of the semiconductor, will result in insulator-like behavior. Furthermore, if the semiconductor quasi-insulator is well chosen and well behaved, the transistor operation should be identical to ideal MISFET operations. Details of the HIGFET are discussed later in this work.

From a historical perspective, the HIGFET is very similar to the early Schottky barrier-enhanced MESFETs. These devices used thin semiconductor layers having large Schottky barriers placed adjacent to the channel layer to enhance the metal-semiconductor gate contact. For example, Ohno and coworkers[19] used a thin layer of InAlAs to enhance the Schottky barrier of a double heterostructure $Ga_{0.47}In_{0.53}As$-channel MESFET. In essence, the devices are similar to the gate structure in a HIGFET since surface depletion is assumed to take place. However, these enhanced Schottky barrier type devices were presumed to operate as depletion-mode MESFETs rather than over the larger dynamic ranges of MISFETs. A second group of devices utilized an undoped lattice-mismatched GaAs gate on a n-$In_{0.53}Ga_{0.47}As$ channel.[20,] Here, the GaAs behaves as a Schottky barrier enhancement with the hope that the large number of defects introduced by the large lattice mismatch do not disrupt performance. GaAs, being well established in MESFETs, was a logical choice because of material quality and known barrier height properties. (Use of a lattice-matched InAlAs layer was considered unfeasible at that time due to poor material growth). Results indicate that the defects are confined to the GaAs/InGaAs interface and do not play a significant role in destabilizing the gate through excessive leakage. HIGFET configurations have been used with pseudomorphic layers with good results.[21]

Other Heterojunction Devices

Other device configurations of notable importance are the semiconductor-insulator-semiconductor field effect transistor (SISFET)[22] and heterojunction field effect transistor (HFET).[23,24] The SISFET, a cross-section is shown in Fig. 1.14(a), is analogous to the polysilicon-gate FET in Si-MOS devices. From the band diagram in Fig 1.14(b), it can be seen that a 2DEG is formed through the inversion of the channel even though the large bandgap semiconductor and channel are undoped. The heavily doped semiconductor at the surface of the device acts as the gate electrode. Of importance here is the resulting threshold voltage dependence on only the work function difference between the gate material and channel, and this is usually close to 0V. This threshold voltage consistency is of great advantage and may be compared to that of a MODFET whose threshold voltage is largely dependent on the thickness and doping of the large bandgap semiconductor layer. Since this layer must often be recess etched, the threshold voltage may vary from device to device and is considered to be highly inconsistent. In addition, the SISFET has an undoped AlGaAs insulator layer compared to a highly doped n^+-AlGaAs layer in the MODFET; it avoids the difficulties seen with DX centers, which are believed to be related to n-type doping centers in AlGaAs.

The HFET, whose cross-section is shown in Fig. 1.15 (a), utilizes an ohmic gate contact to a p-p heterostructure. Located at the p-p heterointerface is a sheet of donor atoms which produces an energy band structure shown in Fig. 1.15 (b). Conduction takes place through an inversion layer formed at the heterointerface. This device is interesting since it creates a barrier between the gate and the electrons flowing in the channel equivalent to the bandgap of the AlGaAs layer, rather than relying on a conduction band discontinuity as have the other devices discussed above.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(a)

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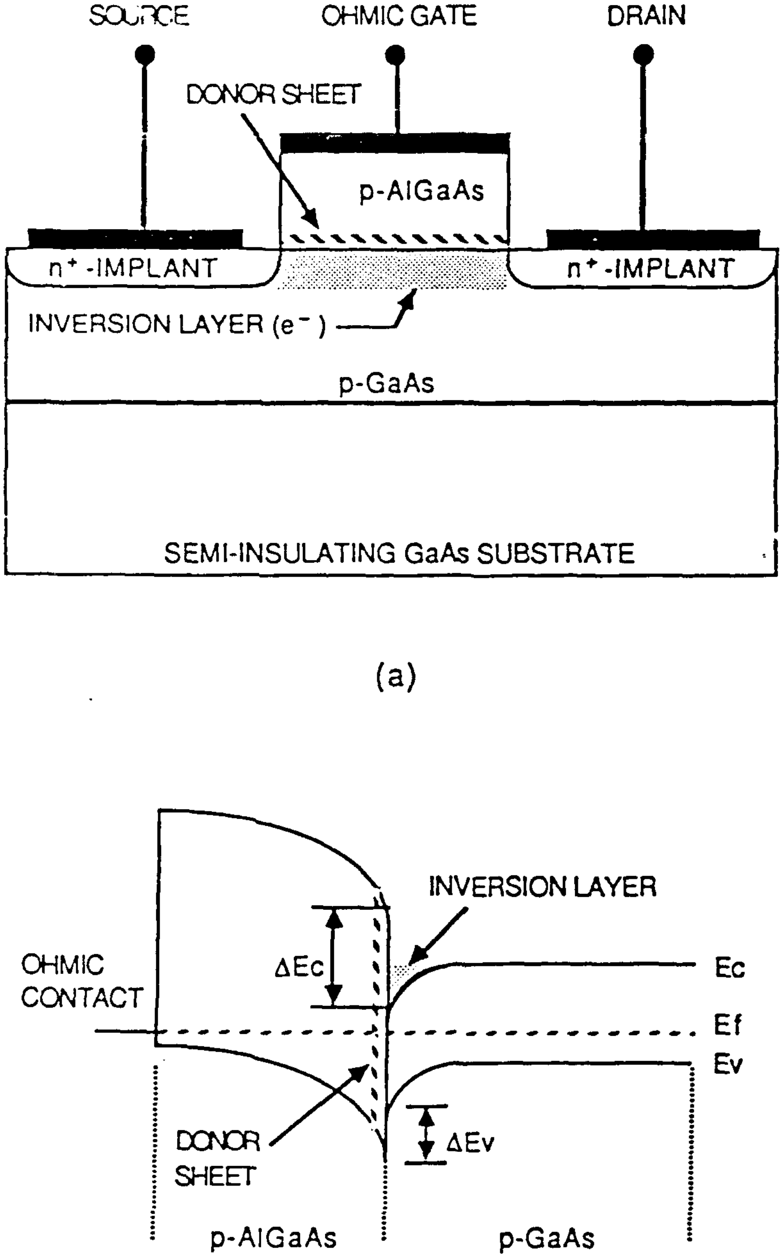
Figure 1.14: Device cross-sectional view and conduction bandedge diagram of the SISFET.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INVERSION LAYER
OHMIC CONTACT
ΔE_c
Ec
Ef
Ev
DONOR SHEET
ΔE_v
p-AlGaAs
p-GaAs

(a)

(b)

Figure 1.15: Device cross-sectional view and energy band diagram of the HFET.

The devices discussed in this section represent many promising device configurations. However, they represent only a handful of possible structures. Variations in selective doping, delta doping, inverted structures, material placement, multilayers, quantum wells, additional enhancing insulators,[25] or combinations of these,[26] can all generate seemingly different devices and operating characteristics. Within the scope of this work, the devices presented in this chapter represent likely candidates to illustrate the potential contributions of using a large lattice-mismatched material system.

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Dislocation Filtering

Introduction

The ability to grow heteroepitaxial semiconductor layers on lattice-mismatched substrates has allowed researchers to investigate new materials and their properties. Unfortunately, one of the drawbacks of growing on mismatched substrates is the potential generation of defects in subsequently grown layers. It is well known that the presence of dislocations may adversely affect the operating characteristics of many devices. Therefore, it is highly desirable to limit or reduce the number of dislocations present in the active regions of devices. As discussed in the previous chapter, slightly lattice-mismatched structures may be grown pseudomorphically, where layers are completely elastically strained with respect to the substrate maintaining coherent interfaces, provided they are kept below some critical thickness. On the other hand, an increase in the interfacial lattice-mismatch and/or an increase in the layer thickness may induce sufficient stress to induce plastic deformation of the layers. This plastic deformation would involve the generation and propagation of dislocations in order to accommodate the increased stress. If one can provide a reasonable efficient means of controlling the generation and/or prevent the propagation of defects, then the device designer may no longer be constrained to using only lattice-matched or near-lattice-matched heterostructures.

Perhaps one of the more interesting problems many researchers have been engaged in is the growth of GaAs on Si. GaAs, and III-V compounds in general, offer many advantages for optoelectronic and electronic device applications. Si has a well established integrated circuit technology and can provide a cheap, mechanically strong, and thermally conductive substrate. Together, one might be able to take advantage of the benefits provided by both materials. The difficulty in growing GaAs on Si is the large lattice mismatch, close to 4%, and the resulting high density of defects (ie. dislocations) introduced by the mismatch which may degrade the desirable properties of the III-V layers grown on the Si substrates. In order to reduce the dislocation density the use of thermal annealing,[1] thermal cycle growth,[2] tilted substrates,[3] and the interposition of strained-layer structures such as strained-layer superlattices (SLS) as buffers have been proposed. Similar methods of reducing the defect density have been applied to lattice-matched as well as lattice-mismatched III-V compounds and their substrates. The work described in this thesis will concern itself only with the use of interposed strained layers between the substrate and active regions. The active region of a device is defined by the layers of material where charge transport occurs under the influence of an applied electric field. The intent of these buffer layers is to limit and reduce the dislocation density which might otherwise degrade the characteristics of the active region. This reduction in the generation or propagation of dislocations by certain layers is referred to as dislocation filtering.

Misfit strain can be used to drive certain types of dislocations out of epitaxial layers. Similarly multiple layers such as strained-layer superlattices can accomplish this effectively by reducing the propagation of dislocations provided these layers are grown within certain criteria. This chapter will deal with the control of defects such as dislocations which are found in ternary compound layers grown on lattice-mismatched substrates. It will include a description of buffer structures which are intended as dislocation filters and present experimental results obtained for InGaAs and InAlAs strained-layer structures grown on GaAs substrates.

An investigation of lattice-mismatched interfaces involves to a large extent an examination of the typical static and dynamic properties of dislocations formed at these interfaces. The (001) interface of the diamond cubic lattice or zinc-blende structure is of primary importance because this is the main substrate orientation available in wafers for device applications. Si and Ge are typical diamond-cubic lattices and III-V semiconductors are representative of the sphalerite or zinc-blende structure. Both Si and Ge are examples of covalent crystals, while the III-V compounds have partly ionic and partly covalent bonding.

The Cubic Structure

In the case of diamond, Si, or Ge, the space lattice is a face-centered cubic with two atoms per lattice site. These are located at 0,0,0 and 1/4,1/4,1/4. A schematic of a typical lattice is shown in Fig. 4.1(a). Each atom is tetrahedrally bonded to four nearest neighbors. Perfect dislocations will lie along the $<1\,1\,0>$ direction with a 0° or 60° orientation to a Burgers vector of $1/2<1\,1\,0>$. Two types of dislocations may be produced, belonging either to the glide set or shuffle set, depending on which plane the fault occurs[4]. Figure 4.2 shows a $(0\,1\,\overline{1})$ projection of the diamond-cubic lattice showing the $(1\,1\,1)$ glide and shuffle planes. In either case, dangling bonds are formed at the dislocation core and the dislocation energy may be altered by bond reconstruction, such that dangling bonds reform with one another to maintain the tetrahedral shape. The presence of dangling bonds and bond reconstruction affects the dislocation core energies and its structure which in turn results in the dislocation being electrically active in some form. This is why most dislocations are undesirable in the

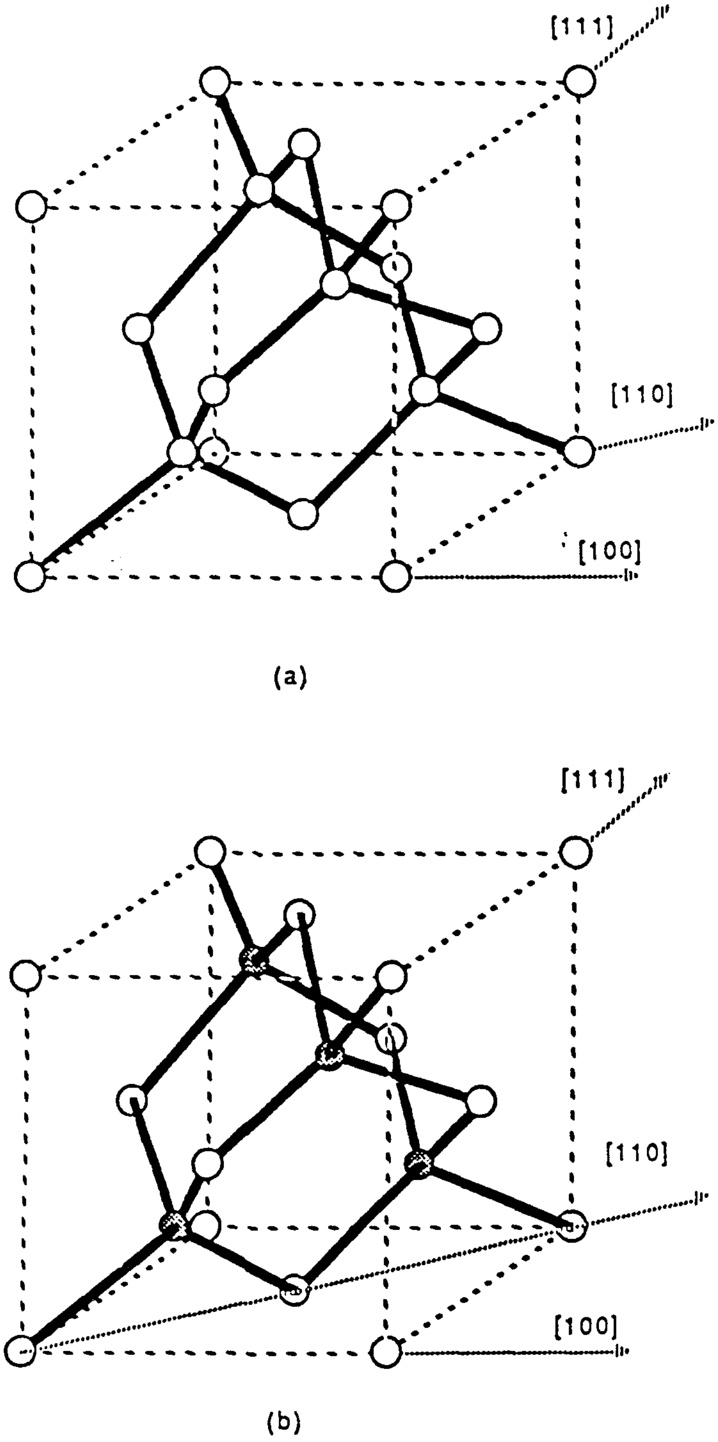

[111]
[110]
[100]
(a)
[111]
[110]
[100]
(b)

Figure 4.1: The unit cell and important crystallographic directions are shown for: a) the diamond-cubic structure, and b) the zinc-blende or sphalerite structure.

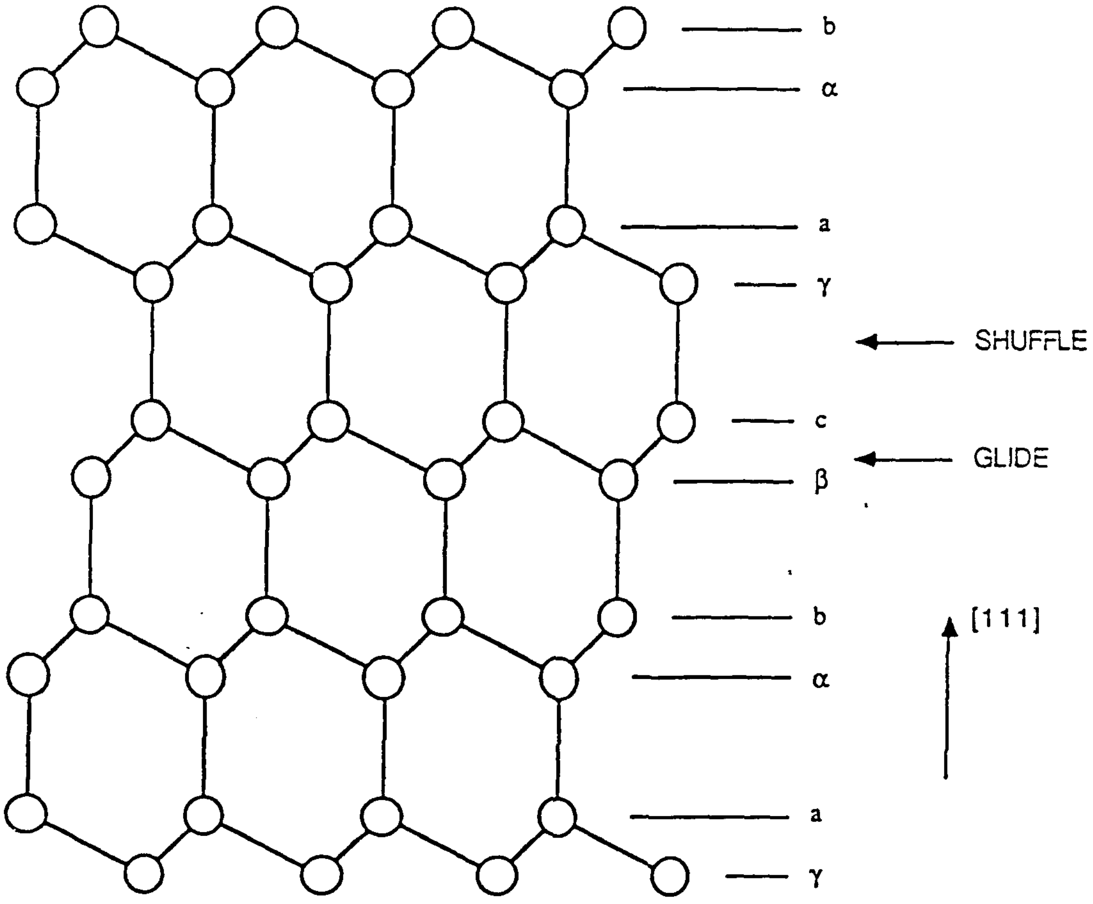


Figure 4.2: A $(0 1 \bar{1})$ projection of the diamond-cubic lattice indicating the $\{1 1 1\}$ planes stacking sequence and location of the $(1 1 1)$ shuffle and $(1 1 1)$ glide planes.

active regions of many devices.

In III-V Compounds

While the sphalerite or zinc-blende structure (shown in Fig. 4.1(b)) appears similar to the diamond-cubic structure, the defects in epitaxial layers of sphalerite

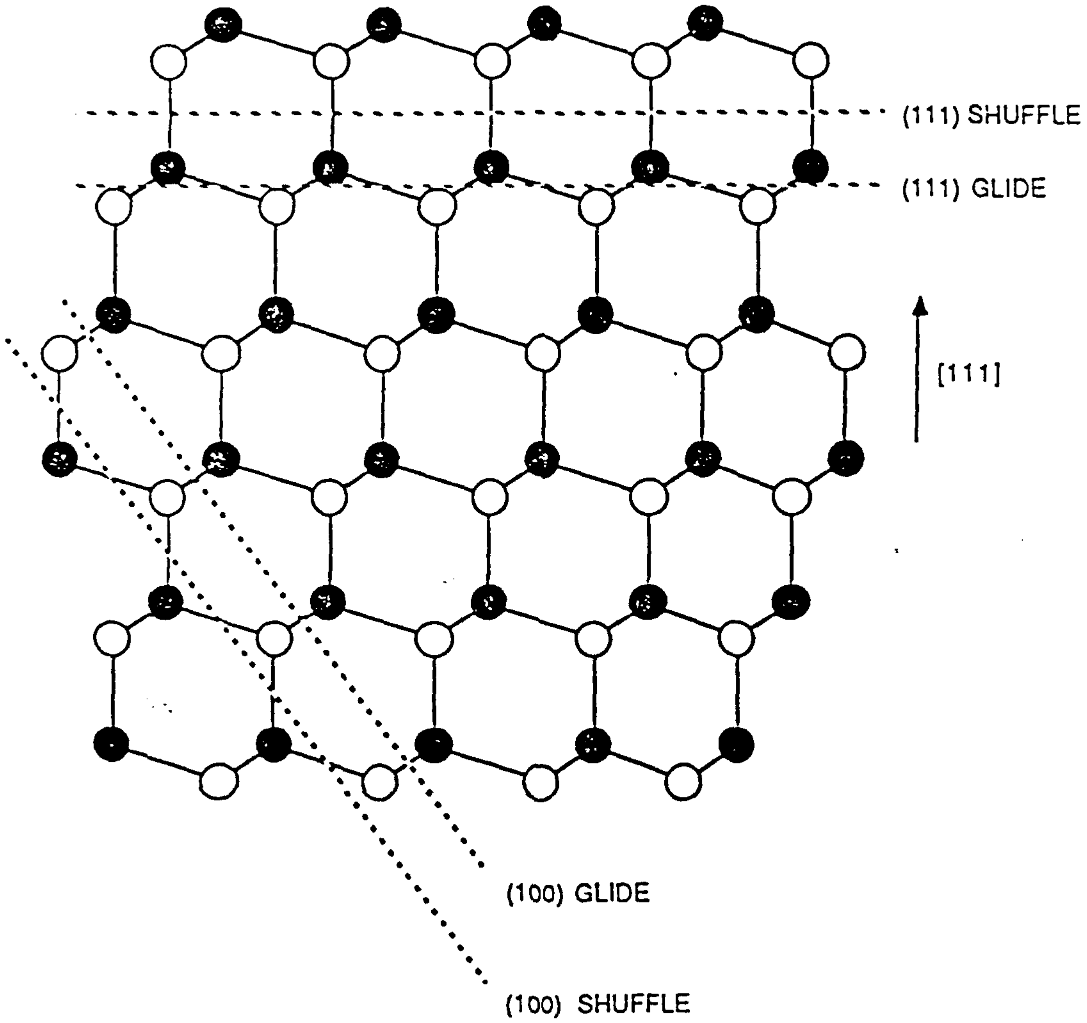


Figure 4.3: A $(0\,1\,\overline{1})$ projection of the sphalerite structure showing the double $\{1\,1\,1\}$ stacked planes and the shuffle and glide planes for the $(1\,1\,1)$ and $(1\,0\,0)$ planes.

structure compounds are more complex. This complexity in the defects can be attributed to the non-centrosymmetricity of the structure and the polytypism of the stacking sequences in some compounds. An example of non-centrosymmetry is the non-equivalence of the $[1\,1\,1]$ direction and the $[\overline{1\,1\,1}]$ direction. Polytypes and polymorphic behavior refer to variations in the stacking sequences of double $\{1\,1\,1\}$ atomic planes. Figure 4.3 shows the $(0\,1\,\overline{1})$ projection of the sphalerite structure. The bβ-cγ.... Also shown in the figure are the glide and shuffle planes for the (1 1 1) and (100) planes. Figure 4.4 shows a similar (0 1 $\overline{1}$) projection of the sphalerite structure in which a (1 1 1) heterojunction exists. The lattice-mismatch results in the formation of a misfit dislocation at the interface. In lattice-mismatched III-V growth, several types of simple dislocations occur. Figures 4.5, 4.6 and 4.7 show an edge dislocation, a 30°-dislocation and a 60°-dislocation, respectively, all corresponding to simple (shuffle) dislocations in the sphalerite structure. The 60° 1/2<1 1 0>-type dislocation is observed to be most dominant. The 60°-dislocation is

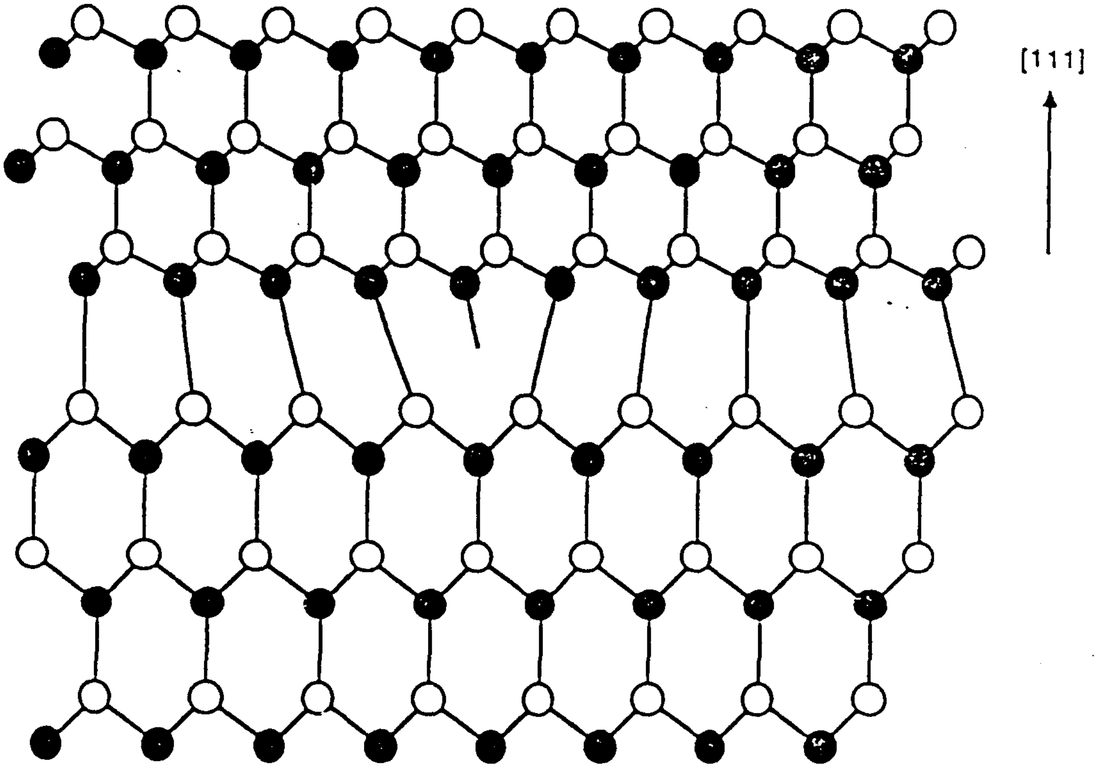


Figure 4.4: A (0 1 $\overline{1}$) projection of a lattice-mismatched (1 1 1) heterojunction where a misfit dislocation has formed.

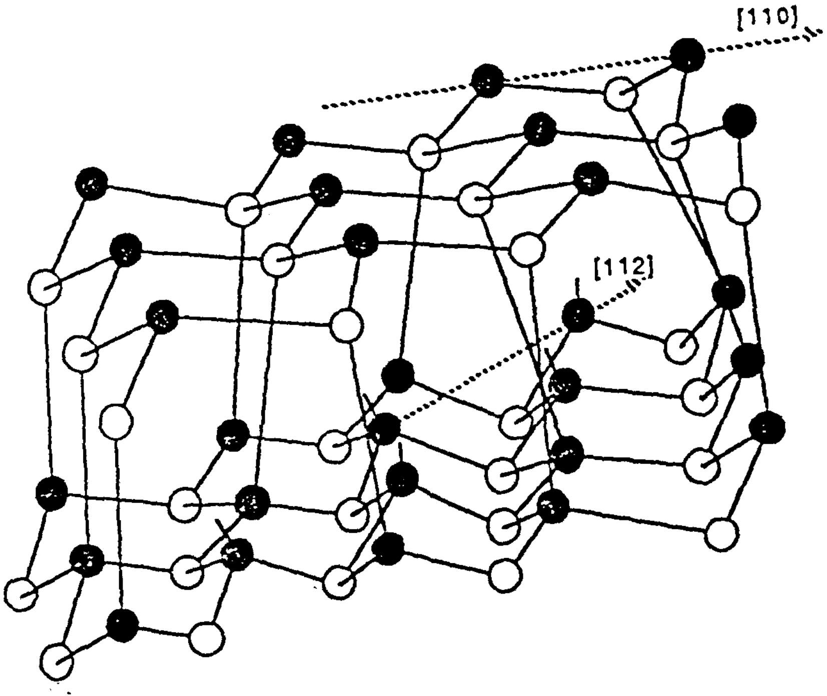


Figure 4.5: An edge dislocation having a {1 1 1} slip plane in the sphalerite structure. The core of the dislocation lies in the <1 1 2> direction with a Burger's vector in the <1 1 0> direction.

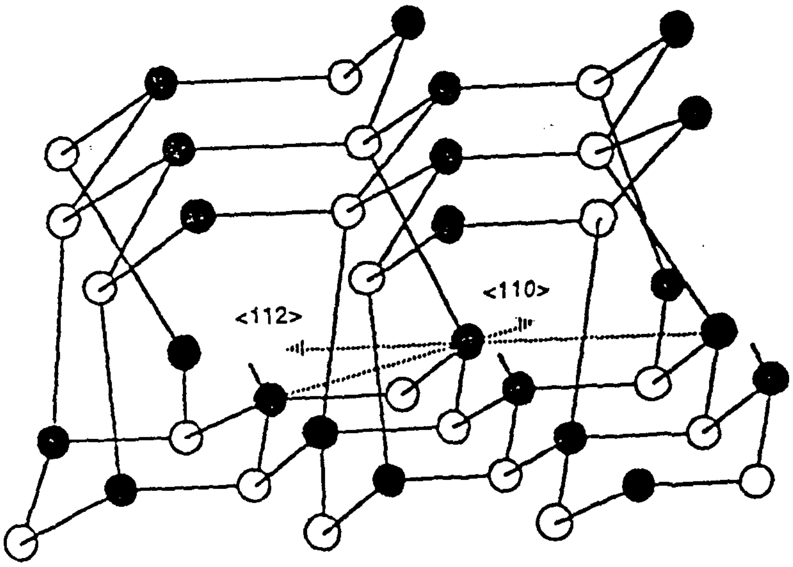


Figure 4.6: A 30°-type dislocation having a {1 1 1} slip plane in the sphalerite structure. The core of the dislocation lies in the <1 1 2> direction and has a Burger's vector in the <1 1 0> direction.

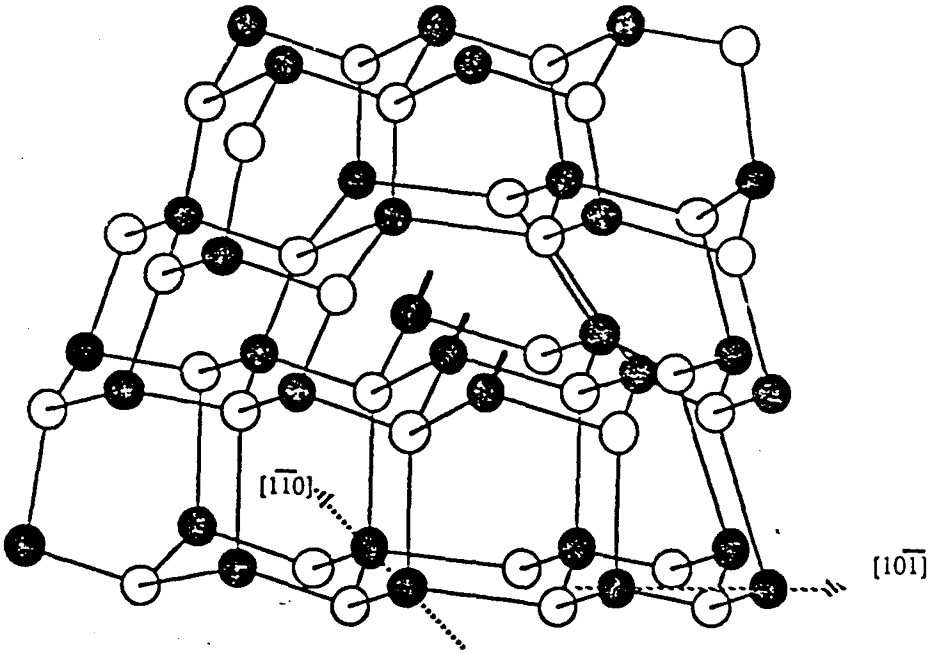


Figure 4.7: A 60°-type dislocation having a {1 1 1}-type slip plane in the sphalerite structure. The core of the dislocation and Burger's vector lie in the <1 1 0> direction.

so-called because of the 60° angle formed between the core of the dislocation, shown as the direction [1 $\bar{1}$ 0] in Fig. 4.7, and the Burgers vector 1/2[1 0 $\bar{1}$]. These dislocations originate on the surface through nucleation and glide or originate from dislocations already present in the substrate.[5] In these simple dislocations, two variations are possible in the sphalerite structure. If the 60°-type dislocation in Fig. 4.7 is taken as an example, one observes that all the atoms with broken bonds in the core of the dislocation are of one type. These are shown as the closed (black) atoms. If these atoms represent atoms of the lower valence element in the compound (ie. Ga in the compound GaAs) then the dislocation is referred to as an α-60° dislocation. Conversely, if the black atoms represent the higher valence element the dislocation is referred to as a β-60° dislocation. The occurrence of the α and β forms in simple dislocations, which correspond to only one form in the diamond-cubic structure, is another example of the non-centrosymmetry in the sphalerite structure. While in the cubic structure the 60°-type dislocations are symmetric, Abrahams and coworkers[6] have observed that the same orthogonal dislocations in InGaP and GaAsP, and hence in the zinc-blende structures, are not equivalent. Similar asymmetries have been observed in the orthogonal 60° 1/2< 1 1 0>-type dislocations in InGaAs/GaAs structures by Kavanagh *et al.*[7] They observe that despite an asymmetry in the densities of dislocation arrays, no asymmetry can be detected in the residual strain in their layers and this suggests that the dislocations are of the same Burgers vector or evenly distributed between two Burgers vectors. Abrahams *et al.* have suggested that the differences between these orthogonal dislocations of like sign may be found in a different rate of nucleation or a different rate of propagation.

Misfit Strain

It has been well established that the presence of a strain field can act on the direction of propagation of a dislocation[8,9,10]. A strain field can exist at a misfit heteroepitaxial interface during the growth of lattice-mismatched epitaxial layers. Misfit strain can drive threading dislocations out of epitaxial films. The process of applying strain energy in the form of mismatched epitaxial layers is dependent on the layer thickness, the mismatch between the layer and substrate, the dimensions of the interface parallel to the growth plane, the orientation of the interface, and growth conditions of the layer, which influences the material properties.

Figure 4.8, after Rozgonyi *et al.*,[11] shows a schematic representation of the effect of interfacial strain on a dislocation propagating from a lower layer. If we consider the lower layer to be that of the substrate, and the upper layer to be a lattice

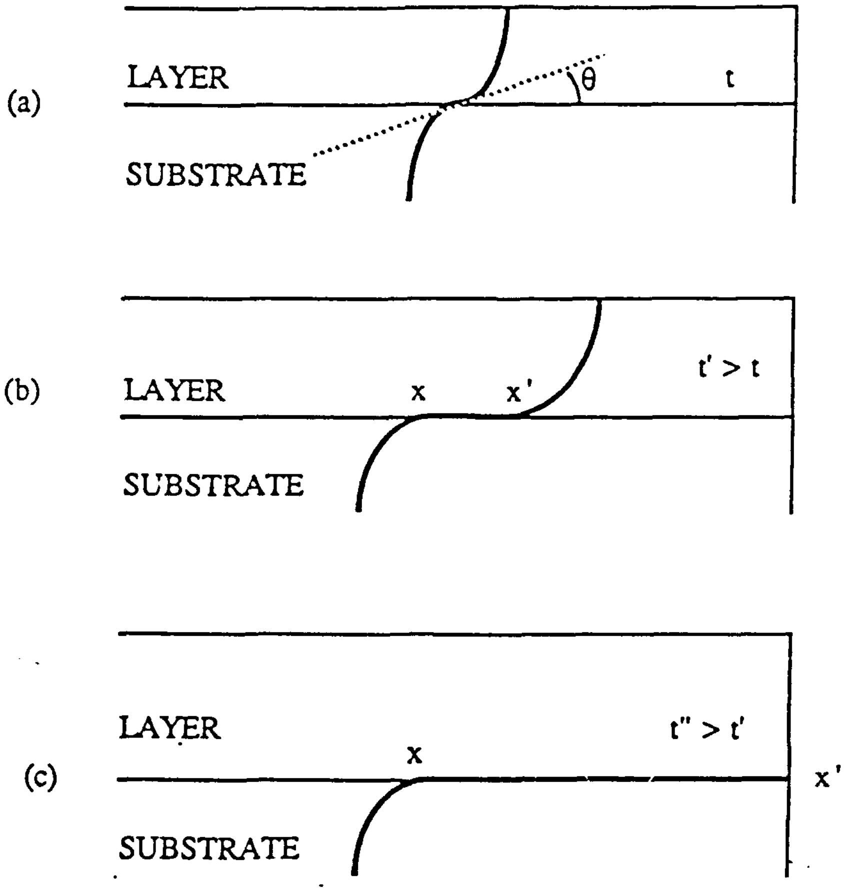


Figure 4.8: Schematic diagram of a dislocation propagating from the substrate. The dislocation (a) bows with an angle θ, (b) glides in the interfacial plane for a finite length x to x', and (c) glides to the edge of the wafer, depending on the thickness of the strained epitaxial layer. (After Ref. 11).

mismatched epitaxial layer of thickness t, then the substrate-layer interface will be coherent provided that the strain is elastically accommodated. The dislocation will become slightly bowed due to the presence of the mismatched interface. As the thickness of the layer is increased, the angle, θ, between the dislocation propagating direction and interface plane is reduced, until the dislocation moves along the interface itself. This is shown in Fig. 4.8 (b) and has a length given as x to x'. At this point the interface is no longer considered to be coherent. If the layer thickness is increased further to t", the dislocation may actually be forced out of the wafer to its edge through glide mechanisms, as shown in Fig. 4.8 (c). Bent dislocations have been known to travel hundreds of microns without disturbance. It should be apparent that the misfit-induced elastic force acting on a dislocation is directly proportional to the layer thickness, the layer-substrate mismatch, and to a constant proportional to the elastic properties of the layer material.

Other factors influencing the removal of threading dislocations include interface orientation. The threading dislocation must experience a glide force in order to be removed. This is directly dependent on the orientation of the interface, since it concerns the angle of the Burgers vector with the slip planes in the layer. For 60°-type dislocations found in zinc-blende crystals grown into (100)-oriented material, this is not a factor. However, not all dislocations are 60°-type and those having a Burgers vector oriented parallel to the interface planes cannot be easily driven laterally by the stress present. Interface dimensions also play a role. The smaller the interface the easier it is to drive the threading dislocation to the edge of the wafer. Work by Fitzgerald[12] has examined the application of reduced growth areas and its effect on dislocation densities. Of greater concern, however, is the layer thickness. While there exists a specific requirement for exceeding a critical thickness in order to begin the formation of misfit dislocations which would remove threading dislocations, it is also necessary to curb the formation of other dislocations or the multiplication of dislocations already present. The thickness must be limited to a magnitude close to that which can generate misfit dislocations, but not greater values so as to generate dislocation half-loops from the growth surface. The formation of half-loops is also a result of the misfit strain in the layer. Furthermore, any perturbation which may increase the local stress increases the probability that nucleation of dislocations may take place. Local induced stresses can originate from defects already present, cracks, high surface steps, or particulate precipitation on the surface. The technique employed in growing strained-layer heterostructures must include care in surface preparation and control during layer growth so as to inhibit such problems from occurring.

While it may be evident that one layer can remove threading dislocations, it is to be expected that multiple layers can be even more effective at removing dislocations. The application of multiple layers improves the chances that a physical imperfection found in one layer would not be found in other layers thus increasing the probability that a dislocation is removed. Again, as with single mismatched layers, multiple mismatched layers have specific requirements and considerations, which will be made apparent in the next section.

Strained-layer Superlattices

Strained-layer superlattices (SLS) involve the application of multiple alternating layers with different lattice constants which set up an alternating strain field intended to remove dislocations. Ideally the lattice constants of the individual layers alternate and the strain fields are opposed to one another; one layer is in compression and the other in tension, such that each layer is accommodated by elastic deformation. The term superlattice is defined in the crystallographical sense to indicate a periodic variation in structure. This term should not be confused with electronic or optical definitions which separates periodic structures into two categories, superlattices and quantum wells. Crystallographically, both quantum wells and superlattices are periodic structures and are therefore defined under the general term of superlattices. Such will be the case used herewith. Matthews and Blakeslee[10] first proposed using GaAsP/GaAs SLS to block the propagation of threading dislocations found in GaAs substrates. Using this concept, Bedair and coworkers[13] demonstrated dislocation reduction by using an InGaAs/GaAs SLS buffer layer, provided that the SLS thickness did not exceed a critical value. Tischler *et al.*[14] circumvented the problems of an overall critical thickness limitation by using a GaAsP/InGaAs SLS whose average weighted lattice constant was matched to that of the GaAs substrate and obtained a reduction in the dislocation density. Shinohara *et al.*[15] have used an AlAs/GaAs SLS to achieve similar results. SLS grown as dislocation filters have been used extensively in the heteroepitaxial growth of GaAs on Si. For example, Nishimura and coworkers[16] have observed a reduction in dislocations traversing InGaAs/GaAsP SLS grown on GaAs layers which were deposited on Si substrates. The properties of dislocation filtering have also been studied using growths of deliberately incoherent layers. Gourley *et al.*[17] have examined $In_xGa_{1-x}As/In_yAl_{1-y}As$ SLS on $In_zGa_{1-z}As$ buffer layers grown specifically to study the effectiveness of certain SLS structures in filtering dislocations. Similar observations have been made on $InAs_{1-x}Sb_x/InAs_{1-y}Sb_y$ SLS on $InAs_{1-z}Sb_z$ by Biefeld[18].

The quality of dislocation filtering can be determined using a number of techniques. Among these are photoluminescence (PL) spectroscopy, etch-pit-density (EPD) studies, transmission electron microscopy (TEM), electron beam induced current (EBIC) measurements, and Hall measurements made on the active layers grown on top of the SLS structures. Photoluminescence studies use PL microscopy techniques in which relatively large areas may be illuminated simultaneously to obtain areal information. Photoexcited carriers in direct bandgap III-V semiconductors recombine radiatively with high efficiency except at defects, thus misfit dislocations provide strong nonradiative recombination sites which will appear as dark lines on a spatial image of a photoluminescence topograph. Similarly, the peak PL intensity in standard PL spectra is reduced if the SLS structure, which can be considered a series of quantum wells, contains dislocations. In addition, a strong shift in the peak energy can be related to a change in energy gap which, in turn, may be related to lattice relaxation induced by dislocations. Etch pit density (EPD) studies provide a method of counting dislocations. Although not a precise measure of the dislocation density, the density of etch pits has been correlated qualitatively with the density of dislocations. The EPD method depends on obtaining an anisotropic etch which etches different lattice orientations at different rates. Defects, which propagate to the surface moving along different crystallographical orientations, will become delineated by the preferential etch and appear as pits. Transmission electron microscopy (TEM) permits direct observation of the material in either plane or cross-sectional view. Its usefulness is limited by the very small sample area, orientation, and method of sample preparation which may, itself, create or eliminate dislocations.

Typical SLS structures use alternating strains to force a threading dislocation to become a misfit dislocation which then propagates to the edge of the wafer. Many results show that although most threading dislocations may be removed by the first few interfaces, several interfaces are necessary. The SLS is also effective at removing dislocations along its entire thickness if dislocations are continuously generated by residual strain. The advantage of using a superlattice as a dislocation filter is that the coherency strain of alternating layers give rise to stresses which aid the motion of a dislocation through one of the materials but opposes its motion through the other. If the stress in one layer drives the threading dislocation into an obstacle, the stress in the next layer will drive the same dislocation away from the obstacle, eventually driving the dislocation out.

Effect of the Layer Thickness

In order for the SLS to be effective as a dislocation filter, it, itself, must not generate dislocations. The efficiency by which a SLS removes dislocation is then dependent on the effective strain between the individual layers of the SLS, the thicknesses of the individual layers, the total average strain of the SLS as a whole with respect to the substrate, and the total thickness of the superlattice as a whole. Hull and coworkers[19] have shown that the stability of the SLS requires the consideration of two critical thicknesses. The first is related to the thickness of the individual layers and the second is related to the overall thickness of the SLS structure. Clearly the individual layers must have a thickness less than the critical thickness discussed in chapter 3, else they will become non-pseudomorphic with one another. The superlattice as a whole is a slightly more complicated case. To begin, consider only a simple SLS structure utilizing two alternating layers, A and B, of n repetition placed directly on a substrate as shown in Fig. 4.9. First, the elastic strain in an unrelaxed SLS must be considered as the superposition of two strain fields. The first is the oscillating strain field due to the alternating individual layers of the superlattice. Second, is a steady uniform strain field which represents the average strain field present between the substrate and the SLS as a whole. The magnitude of the average strain field may written as

$$s_{avg} = \frac{(s_A d_A + s_B d_B)}{(d_A + d_B)}, \tag{4.1}$$

where s_A and s_B are the strain components in the plane of the interfaces with respect to the substrate, and d_A and d_B are the thicknesses of layer A and B, respectively. If the SLS as a whole undergoes relaxation due to the formation of dislocations, or if the superlattice structure is grown with an average lattice constant matching that of the

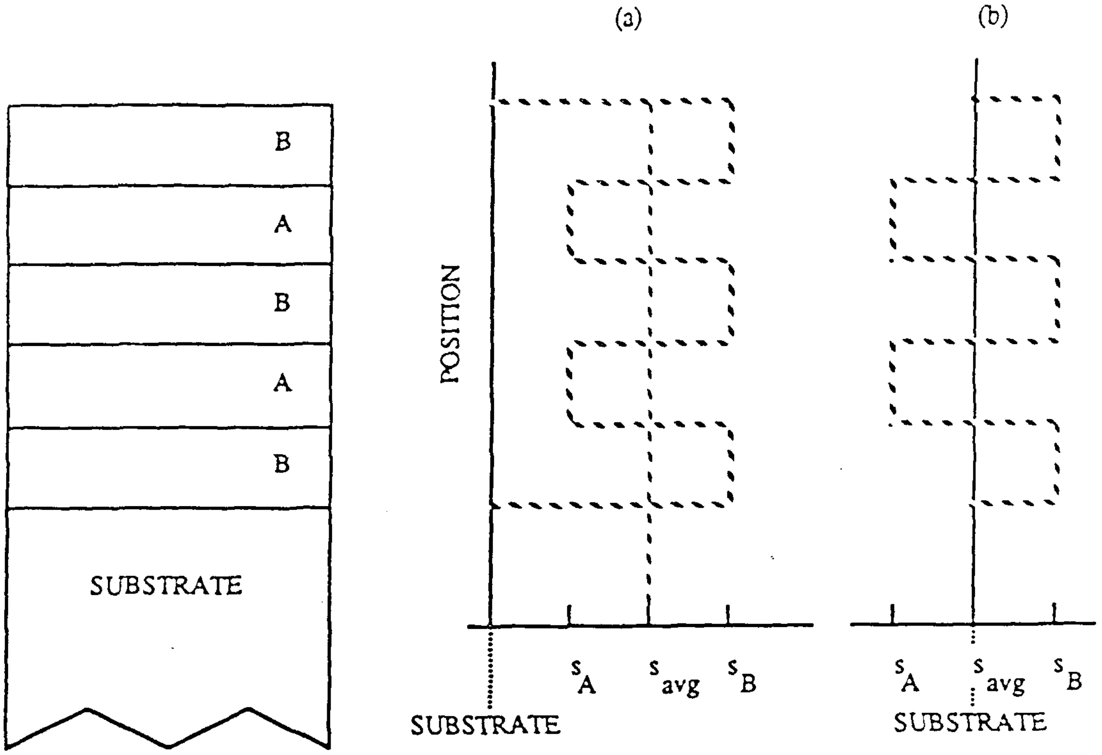


Figure 4.9: Schematic diagram showing the strain field in (a) pseudomorphic superlattice and (b) a totally relaxed or lattice matched superlattice with respect to the substrate. In (a) the total strain field is shown by the dashed line and the uniform or average strain field is shown by the dotted line. In (b) the uniform or average strain field is matched to the substrate. (After Ref. 19).

substrate, then s_{avg} becomes zero, as shown in Fig. 4.9 (b). The maximum strain energy related to the SLS is the same as the total strain energy of a uniform layer of the same total thickness as the SLS having a strain equivalent to the average strain weighted over the relevant elastic constants and layer thicknesses. In other words, the analysis of the SLS may be simplified by considering it to be a uniform layer of the same thickness having a strain, s_{avg}, with respect to the substrate. With this simplification, the SLS as a whole must have a thickness less than the critical thickness of an equivalent uniform layer and may follow the criteria established in chapter 3. Work by Fritz *et al.*[20] and

Andersson *et al.*[21] on $In_xGa_{1-x}As/GaAs$ superlattices show that the critical thickness of the SLS is in good agreement with the theoretical expression proposed by Matthews and Blakeslee[10] for uniform layers. If the SLS has two alternating layers whose weighted strains are equal but opposite with respect to the substrate, then it is possible to grow the SLS with infinite thickness and remain dislocation free, provided the individual layers do not exceed their own critical thicknesses.

While it is clear that the superlattice structure must be designed with thicknesses less than the critical thicknesses, it is also necessary to consider a threshold thickness, from which dislocation filtering begins. Similarly there is a minimum period or repetition for which a SLS will be an effective filter of dislocations. Yamaguchi *et al.*[22] has calculated a threshold misfit force by extrapolating from his data the misfit force at which the relative dislocation density is unchanged by the presence of the SLS. This misfit force is determined to be $5x10^{-5}$ dyne and is independent of the SLS chosen. The SLS may thus be optimized by maintaining thicknesses greater than the threshold thickness for dislocation reduction but less than the critical thickness to prevent dislocation generation.

Various studies have been made to determine the effect of the number of periods a SLS has on its filtering ability. Fritz *et al.*[23] has determined that the efficiency of the filtering is dependent on the mismatch and layer thickness with increased mismatch providing better efficiency, as long as it meets the SLS criteria for dislocation filtering. They have observed for the $In_{0.2}Ga_{0.8}As/GaAs$ SLS on GaAs substrates, that 3 to 6 periods are required for attaining high Hall mobilities while 6 to 9 periods are required to remove visible dislocations in PL micrograph images. Soga *et al.*[24] have observed that for $GaP/GaAs_{0.5}P_{0.5}$ and $GaAs_{0.5}P_{0.5}/GaAs$ SLS grown on Si substrates that 10 periods are necessary to maximize PL peak intensities. Finally, Cao and coworkers[25] have observed through EPD studies that 15 periods are needed to minimize the EPD in $GaAs_{0.54}P_{0.46}/GaAs_{0.66}P_{0.34}$ SLS grown on various buffer structures grown on Si substrates. The EPD approaches a minimum value but does not decrease with a further increase in SLS periods. Cao *et al.* presumes this to be due to the SLS ability to affect only certain dislocations with specific Burger's vectors. El-Masry and coworkers[26] have observed that in cases of high dislocation densities the SLS has a finite capacity for blocking the dislocations. It appears that the higher the dislocation density, the higher are the chances of dislocation-dislocation interactions, and as a result the greater the probability that dislocation multiplication will occur and dislocations will thread through the layers.

Lattice-matched (unstrained) Superlattices

Lattice-matched or unstrained superlattices have also been observed to be effective dislocation filters[17]. These superlattices are composed of alternating lattice-matched layers. Since the individual layers are lattice-matched, they are unstrained with respect to one another. Thus the filtering action of the superlattice is not dependent on the presence of a misfit strain between individual layers. Instead, it is believed that the elastic constant discontinuities present between the alternating layers are responsible. The differences in elastic properties between adjacent layers forces the dislocation to more easily thread through a "compliant" layer but experience greater difficulty in threading through a "stiffer" layer. In other words, it becomes more energetically favorable for the dislocation to lie in one layer if the elastic moduli vary radically between layers. The advantage of the lattice-matched superlattice is its less stringent growth requirements. It does not have to be limited in total thickness or in individual layer thicknesses. It is also effective at removing dislocations which would not otherwise experience glide forces found in SLS structures. Unfortunately, lattice-matched structures have their limitations. They are not as effective as dislocation filters compared to strained-layer superlattices since they must rely on the available lattice-matched materials and the associated differences in elastic constants between those layers. The lattice-mismatch in a SLS allows larger strain fields to be present improving dislocation filtering. Furthermore SLS structures are typically used when working with artificial lattice parameters, where lattice-matching is not possible or would not be effective enough.

Modulation-doped Superlattices

Modulation doping in superlattices has also been proposed as a method of enhancing dislocation filtering. Shinohara[27] has demonstrated the use of an AlAs-GaAs SLS with modulation doping where the doping enhances the filtering action of the SLS. It is believed that dislocation bending is increased due to the interaction of the dislocation with electric charges. From Sec. 4.2.1, dislocations may have a considerable charge associated with them. Modulation doping of a SLS with Si results in spatial separation of the negative electrons and positive ionized donors. In effect an alternating electrical field, like the strain field, is present. Impurity dislocation locking is not considered to be a cause since the doping concentration is too low to cause the lattice distortion needed to lock dislocations.

Other Buffer Considerations

The application of strained-layer superlattices alone is not necessarily the most effective manner in which to remove the defects associated with a large lattice-mismatch. If the lattice-mismatch is large enough micro-cracks may form as well. Micro-cracks, unlike some dislocations, cannot be removed by strained-layers. To prevent microcracks it is often necessary to compositionally grade the buffer either using abrupt step grading or a continuous linear form of grading. Soga *et al.*[24] have interposed AlP and AlGaP steps to grade from the Si substrate to the GaAs epilayers. Olsen *et al.*[8] have already shown that dislocations may be confined to graded regions by using an abrupt compositional step in both step-graded and continuous-graded samples. Furthermore, graded buffers may enhance the relaxation of the lattice constant where artificial lattice constants are required. Most SLS structures use a buffer between the substrate and itself. The buffer acts to stabilize the lattice constant with which the SLS equilibrium lattice constant is matched to.

Relaxation

An artificial lattice constant which may be desirable is attainable only if the material undergoes a proper lattice relaxation. Relaxation of the lattice must be achieved through the generation of dislocations and not through other defects such as microcracks. Ideally one would prefer the relaxation to take place only through the generation of misfit dislocations which are confined to the misfit heterointerface. However, the ideal is rarely the case. Tsao *et al.*[28] has addressed the issue of material plasticity, where the stability and metastability of strained layers is examined. It is concluded that films may be grown having stresses greater than that required for plastic deformation but do not become strain relieved, or that films which are strain relieved may still be partially metastable. Dodson[29] has addressed the process of relaxation and cites Taylor work-hardening as a process involving dislocation-dislocation interactions which interferes with further relaxation. Incomplete relaxation of the lattice parameters toward the desired artificial lattice constant may result in the generation of dislocations at undesirable regions in the device structure. Cao *et al.* [25] observed that the SLS, although functioning, failed to inhibit dislocations if a residual strain existed in the superlattice and resulted in dislocation generation rather than reduction when further top layers were grown. The residual strain in the SLS occurs when the in-plane lattice constant of the underlying buffer is not the same as the equilibrium in-plane lattice constant of the SLS. The equilibrium in-plane lattice constant of the SLS is the value it would take if the SLS were free-floating, i.e. independent of the underlying buffer or substrate. In order to relax the lattice constant prior to growing the superlattice filter, several continuous-graded buffers were interposed. Hyperlinear-, linear- and sublinear-graded buffers, as shown in Fig. 4.10 were used with linear-graded buffers having the best performance. Sublinear-graded layers appear to have too great a

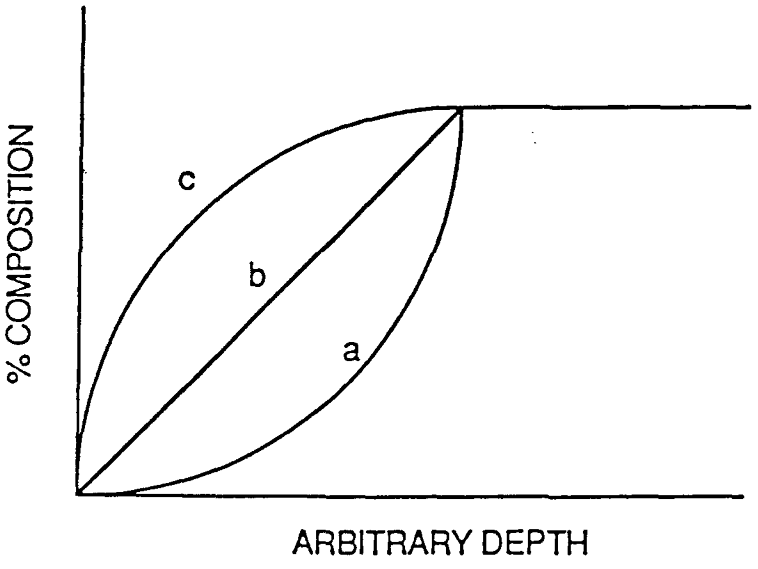


Figure 4.10: Three types of graded layer profiles: (a) sublinear, (b) linear, and (c) hyperlinear.

residual strain while hyperlinear-graded layers result in microcracks and excessive defect formation. In order to remove all residual strain in the SLS, an overshoot in the linear-graded layer was introduced. Figure 4.11 shows a composition versus depth profile of the $GaAs_{1-x}P_x/GaAs_{1-y}P_y/GaAs$ buffer structure with an overshoot designed in the linear-graded layer in order to fully relax the lattice constant prior to the SLS region.

Biefeld *et al.*[30] have investigated constant composition, step-graded, and continuous-graded buffer layers, examining the residual strain found in SLS grown over these buffers and the density of dislocations and cracks formed. They have

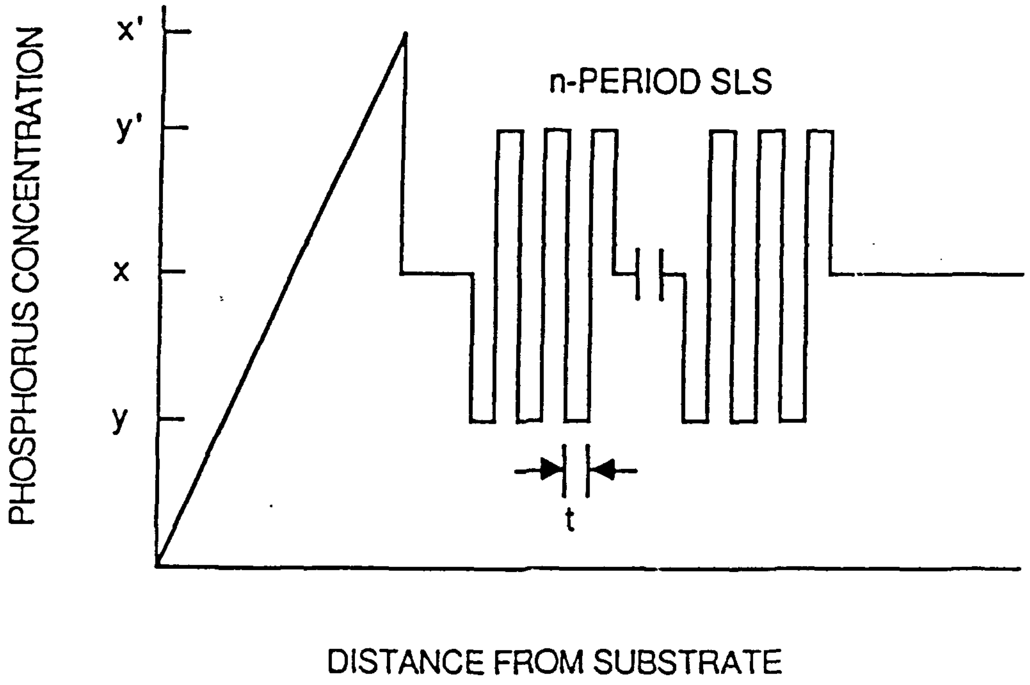


Figure 4.11: Structure consisting of a linear graded layer having a final composition x', a $GaAs_{1-y'}P_{y'}/GaAs_{1-y}P_y$ SLS, and a constant $GaAs_{1-x}P_x$ layer. The SLS structure has individual layer thicknesses, t, and n periods. (After Ref. 25).

determined that thick linear-graded buffer layers provide the greatest strain relief. Furthermore, the presence of residual strain in the SLS will determine whether or not dislocation generation will take place in the structure. Crack formation can be controlled by careful grading of the buffer. If not enough dislocations are allowed to form in the graded buffer, thus preventing enough strain relief, then cracks may form when the critical thickness for crack formation is exceeded.

Experimental Work and Discussion

Introduction

This section will discuss the steps necessary to establish a strained-layer buffer structure which relieves strain and spatially confines dislocations within itself producing an effective lattice constant different from that of the substrate. The purpose of the buffer structure is to isolate the active regions of the device from the substrate and prevent any defects, which may affect the electrical properties of the active region, from propagating into the active regions from any substrate/epilayer interfaces having large lattice mismatches. Chapter 5 will examine in depth the heterojunction insulated-gate field effect transistor (HIGFET) which is the device chosen to demonstrate the applications of a strongly lattice-mismatched material system. It is the objective of this chapter to illustrate the importance of first building the necessary foundation, i.e. the buffer, onto which the active device will be built. Regardless of how well designed the active portion of the device is, without a well conceived and stable buffer structure the completed device or circuit will be doomed from the start.

The heteroepitaxial structures considered here utilize various compositions of the ternary compounds $In_xGa_{1-x}As$ and $In_yAl_{1-y}As$ grown by molecular beam epitaxy

(MBE) on GaAs substrates. The active channel of the device is chosen to have a composition of $In_{0.30}Ga_{0.70}As$ and the buffer must be designed to support this channel. $In_{0.30}Ga_{0.70}As$ has a 2.3% lattice mismatch relative to GaAs. This suggests that any structure composed of $In_{0.30}Ga_{0.70}As$ grown directly on a GaAs substrate or a GaAs lattice-matched buffer will contain a large number of dislocations if it is grown to any appreciable thickness. The calculated critical thickness for a 2.3% lattice mismatch ($In_{0.30}Ga_{0.70}As$ on GaAs) is about 145Å based on the People and Bean model and only 65Å based on the Matthews and Blakeslee model. Such thickness limitations represent a major impediment in the design of pseudomorphic $In_{0.30}Ga_{0.70}As$ layers grown directly on GaAs for transistor device purposes. Furthermore, an increase in the In content, which is of likely interest for increasing the electron mobility and saturation velocity, will not be feasible. Consideration must be given to buffer structures which will facilitate the growth of the $In_{0.30}Ga_{0.70}As$ channel layer without the presence of defects which would affect the channel parameters. To accomplish this, two buffer structures have been considered. The first is a buffer structure whose strain-relaxed lattice constant is equivalent to that of unstrained $In_{0.30}Ga_{0.70}As$. The second utilizes a structure whose strain-relaxed lattice constant is equivalent to that of unstrained $In_{0.15}Ga_{0.85}As$. The first buffer structure creates an artificial lattice constant such that the growth of the $In_{0.30}Ga_{0.70}As$ channel will be in an unstrained state, lattice matched to the buffer structure beneath it. In the second structure, the $In_{0.30}Ga_{0.70}As$ channel layer will be elastically deformed, in compression, with respect to the buffer. However, since the buffer represents a new pseudo-substrate of a different artificial lattice constant, the lattice-mismatch between the $In_{0.30}Ga_{0.70}As$ channel and substrate is reduced to 1.15% compared to the original 2.3%. This change allows thicker pseudomorphic layers to be grown, in this case, channel layers of thicknesses acceptable to the standards set for the design of the HIGFET device.

Experiment and Discussion

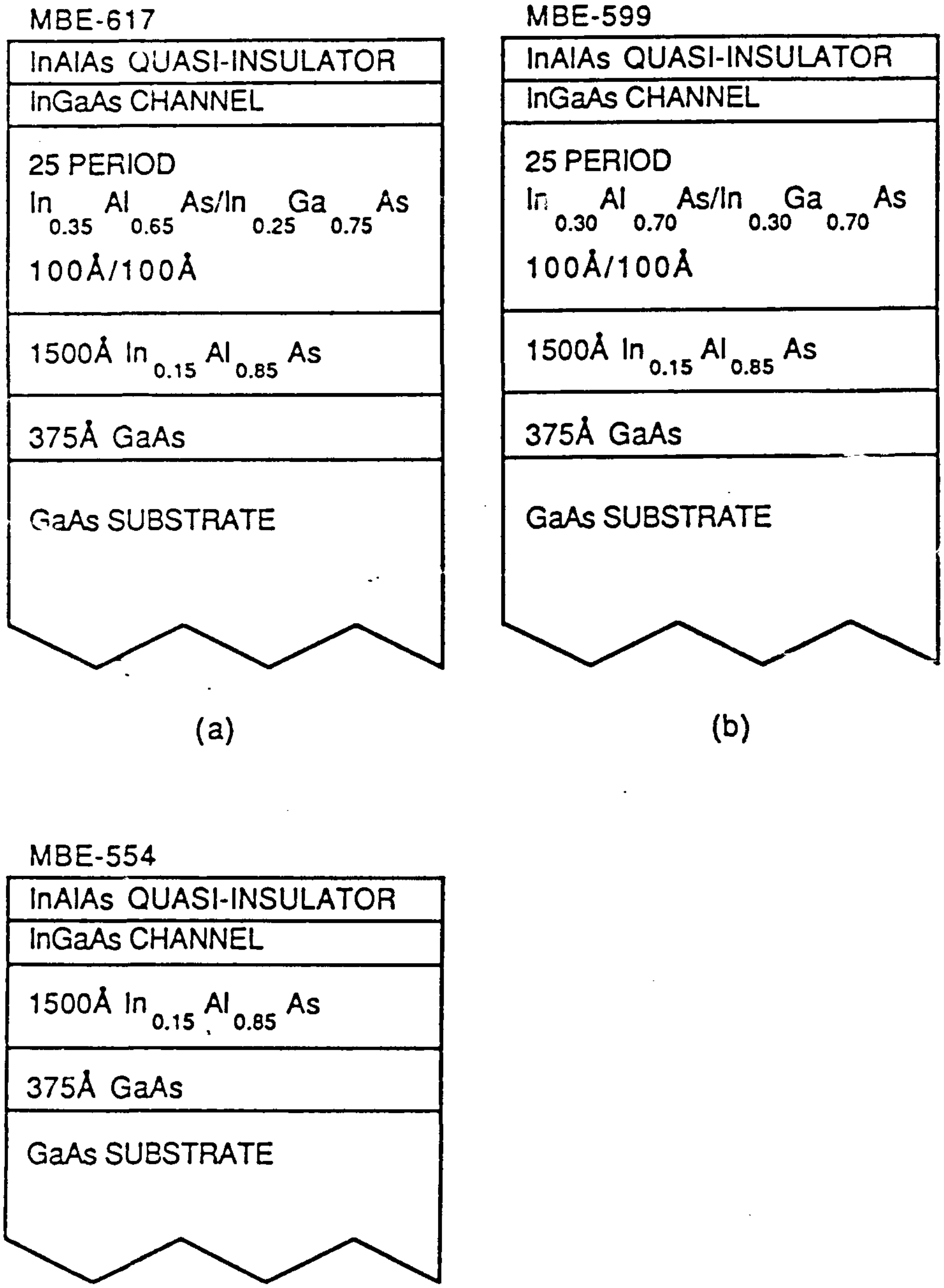
The experiment and discussion section is divided into two parts. The first part relates work on the buffer whose unstrained lattice constant is equivalent to that of $In_{0.30}Ga_{0.70}As$. The second part relates work on the buffer whose unstrained lattice constant is equivalent to $In_{0.15}Ga_{0.85}As$.

The primary purpose of the buffer is to prevent the propagation of dislocations generated at the substrate/ buffer interface or within the buffer layers from reaching the active regions of the structure. Whether accomplished by preventing the formation of threading dislocations or by confining formed threading dislocations within the buffer, the interposed buffer structure is considered to have has accomplished its purpose if, in spite of the lattice mismatch, the density of defects in the active layers of the device are reduced to negligible values; the buffer may be referred to as a dislocation filter. The buffer structure must also be designed so that the relaxation of the compressive strain produces an effective lattice constant supportive of the subsequently grown layers. If not enough relaxation has taken place, the growth of subsequent layers may induce the formation of defects at interfaces adjacent to the active region or within the active region degrading the device performances. The crystalline quality of the active region will also depend on the conditions established for growing high quality heteroepitaxial layers in and on a strain-relaxed buffer. Poor growth in the buffer will probably be reflected by equally poor growth of the active layers. Since good MBE growth is dependent on the quality of the substrate, the growth of a buffer which acts as a pseudo-substrate must be considered to be of equal importance.

An $In_{0.30}Ga_{0.70}As$ Equivalent Buffer

Various $In_{0.30}Ga_{0.70}As/In_{0.30}Al_{0.70}As$ structures were grown on (100)-oriented semi-insulating GaAs substrates by MBE using the standard approach discussed in greater detail in chapter 5. All structures consisted of a buffer, a Si-doped n-type $In_{0.30}Ga_{0.70}As$ channel layer, and an undoped $In_{0.30}Al_{0.70}As$ quasi-insulating cap. These structures were evaluated electrically by means of conductivity and Hall measurements and from I-V characteristics of HIGFETs processed from these layers. X-ray diffractometry was used to confirm the composition of certain layers and transmission electron microscopy was used to estimate the dislocation filtering properties of the buffer structures.

A variety of buffer structures have been examined. All GaAs substrates undergo an oxide desorption at high temperature under an As overpressure in the MBE reactor prior to growth. All buffer structures include an epitaxially grown undoped GaAs layer next to the substrate. This layer is always grown in order to smooth out and establish a high quality growth surface on the GaAs substrate. The simplest buffers consisted of a thick $In_{0.30}Al_{0.70}As$ layer. Other buffers utilized a single step grading consisting of a thick $In_{0.15}Al_{0.85}As$ layer followed by a thick $In_{0.30}Al_{0.70}As$ layer. More complex buffer structures were made which utilized similar layers but included an $In_{0.30}Al_{0.70}As/In_{0.30}Ga_{0.70}As$ or $In_{0.35}Al_{0.65}As/ In_{0.25}Ga_{0.85}As$ SLS. Figure 4.12 show some typical schematic cross-sections of such structures which were grown and their properties evaluated. Thin spacer layers of GaAs, approximately 20Å in thickness, were used in some of the samples. These GaAs spacers were followed by two minute interruptions in the growth sequence, while maintaining an arsenic stable environment, to allow maximum smoothness recovery of the growth surface. As discussed in


MBE-617
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
25 PERIOD
In0.35 Al0.65 As/In0.25 Ga0.75 As
100Å/100Å
1500Å In0.15 Al0.85 As
375Å GaAs
GaAs SUBSTRATE
MBE-599
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
25 PERIOD
In0.30 Al0.70 As/In0.30 Ga0.70 As
100Å/100Å
1500Å In0.15 Al0.85 As
375Å GaAs
GaAs SUBSTRATE
MBE-554
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
1500Å In0.15 Al0.85 As
375Å GaAs
GaAs SUBSTRATE

(a)

(b)

(c)

igure 4.12: Schematic cross-section of three samples utilizing $In_{0.30}Ga_{0.70}As$ equivalent buffers. (a) Sample MBE-617, which uses an $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.75}As$ SLS and a single discrete step grade. (b) Sample MBE-599, which uses an $In_{0.30}Ga_{0.70}As$/ $In_{0.30}Al_{0.70}As$ SLS and a single discrete step grade. (c) Sample MBE-554, which has a buffer consisting of only a single discrete step grade.

Chapter 2, these GaAs spacers are used to improve the rough interfaces caused by three-dimensional growth of InAlAs and InGaAs, which is suggested[31] to occur for these compositions and growth conditions.

The results obtained with these buffer structures are presented in Table 4.1. 5μm gate length HIGFET devices were fabricated using the procedures outlined in chapter 5. The devices were evaluated by examining their I-V characteristics using a transistor curve tracer. The extrinsic transconductance, g_m, derived from these measurements is listed in the table and is considered to be a qualitative indication

TABLE 4.1: Results compiled from conductivity and Hall measurements, and the extrinsic transconductance as determined from the I-V characteristics of HIGFETs fabricated from the structures shown in Fig. 4.12. HIGFETs have $L_g=5\mu m$, $W_g=280\mu m$, and $L_{sd}=16\mu m$.

Sample	Buffer	n (cm^{-3})	μ ($cm^2/V\text{-}s$)	g_m (mS/mm)
MBE-617	with SLS	1.3×10^{17}	2670	87
MBE-599	unstrained superlattice	1.5×10^{17}	250	<1
MBE-554	no superlattice	4.6×10^{17}	420	18

of the effectiveness of the dislocation filtering of the buffer. It is presumed that all aspects of the transistor device and fabrication procedures are identical, such that the measured variations between different structures are due only to the variations in their buffer structures. Van der Pauw test configurations were also fabricated on the same layers. Room temperature conductivity and Hall measurements were made using these samples. Defects which propagate into the channel from a buffer which is a poor dislocation filter are considered to degrade the channel electron concentration and mobility. These measurements are also included in Table 4.1.

The data presented in Table 4.1 and results of other samples not shown here suggest that dislocation filtering is enhanced by using a SLS structure in the buffer. The best device characteristics obtained thus far employ superlattice buffers. When considering different SLS structures, the performance of those structures using $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.85}As$ SLS appear to be superior to those with $In_{0.30}Al_{0.70}As$/ $In_{0.30}Ga_{0.70}As$ SLS. Figures 4.13 and 4.14 show TEM cross-sectional views comparing these two structures. The $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.85}As$ SLS shows better confinement of the dislocations in the buffer than the structure using an $In_{0.30}Al_{0.70}As$/ $In_{0.30}Ga_{0.70}As$ SLS. Different $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.85}As$ SLS buffers were also examined. Using the same overall thickness for the buffer, a 25 period 100Å/100Å $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.85}As$ SLS was compared with a 50 period 50Å/50Å $In_{0.35}Al_{0.65}As$/ $In_{0.25}Ga_{0.85}As$ SLS. The 50 period 50Å/50Å SLS was observed by TEM to have fewer threading dislocations which penetrated the SLS and propagated to the channel layer. This suggests that an increase in the number of strained heterointerfaces may improve dislocation filtering. Furthermore, 50Å layer widths are sufficient to produce a filtering effect without inducing a loss in filtering capability. A decrease in filtering quality is expected if the individual layer thickness is decreased below a threshold thickness as discussed in section 4.4.1 of this chapter.

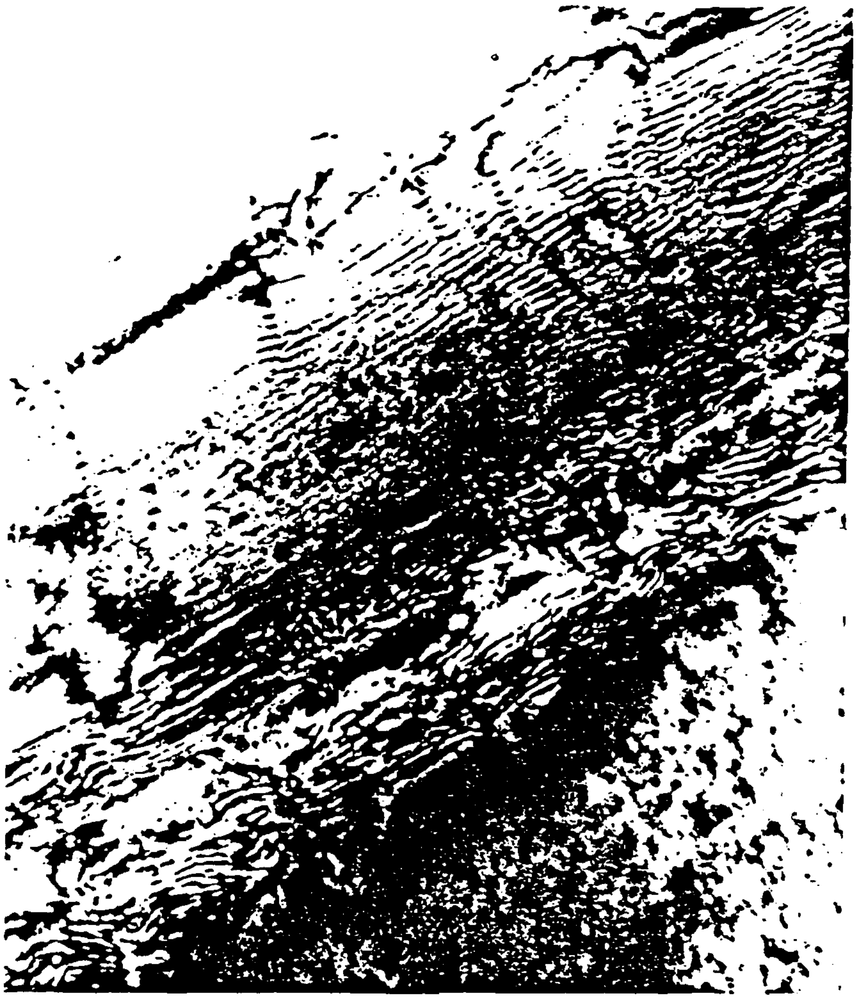


Figure 4.13: Cross-sectional transmission electron micrograph of a buffer structure utilizing an $In_{0.30}Ga_{0.70}As$/ $In_{0.30}Al_{0.70}As$ SLS.

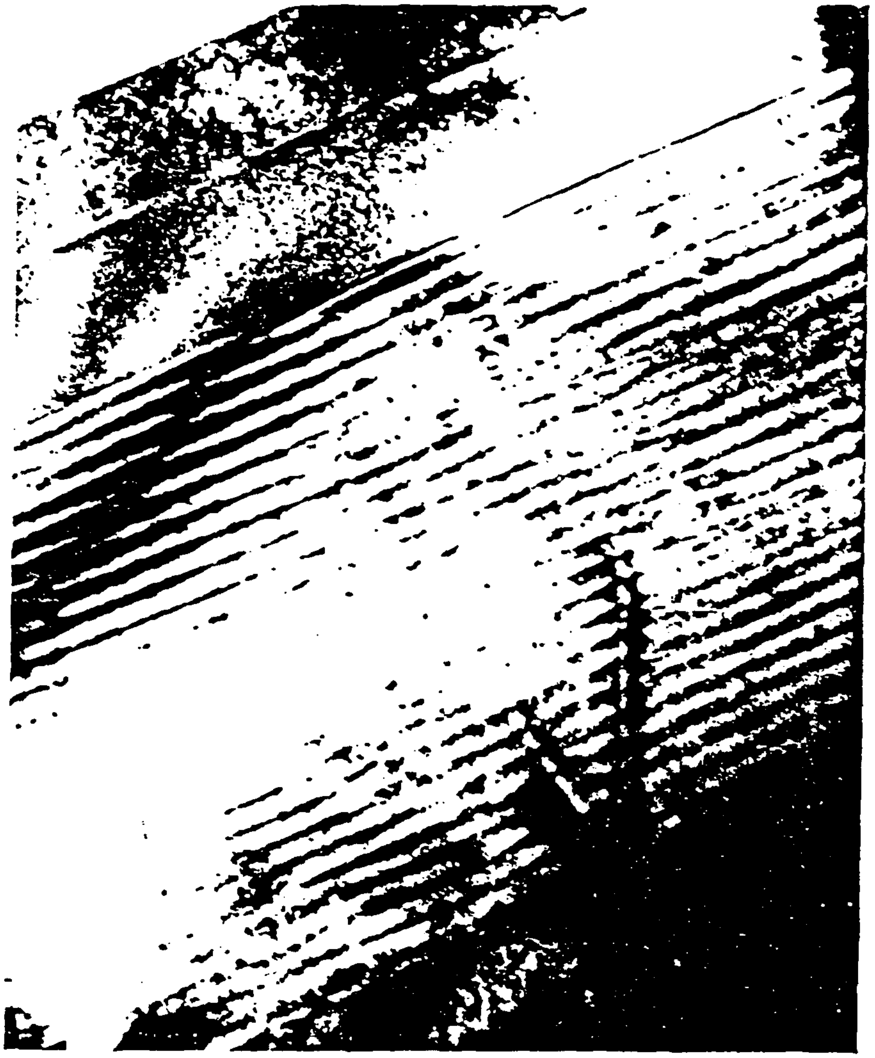


Figure 4.14: Cross-sectional transmission electron micrographs of a buffer structure utilizing an $In_{0.35}Al_{0.65}As/ In_{0.25}Ga_{0.75}As$ SLS.

Samples with GaAs spacer layers and interruptions in growth sequences proved to be moderately superior to those without such spacer layers. It is possible that such spacer layers enhance the quality of the heterointerfaces where they are introduced. A two minute interruption in growth following the deposition of a thin GaAs spacer layer allows the GaAs at the growth surface to relax, redistributing across the surface, creating a smooth interface onto which subsequent layers are grown. The smoothing of the interface will enhance the interface quality about the $In_{0.30}Ga_{0.70}As$ channel layer. In addition, the GaAs spacer layer may prevent interdiffusion between ternary alloys which comprise the heterojunction thus improving the interface and electrical characteristics of the channel layer.

A structure which utilizes a graded buffer leads to superior transistor characteristics. Figure 4.15 shows a schematic cross-section of two samples, one with a graded buffer and one without such grading. The graded buffer consists of a single abrupt step of $In_{0.15}Al_{0.85}As$ situated between the substrate and SLS. A comparison of the two samples is listed in Table 4.2. The improvement in device performance when using a step grade suggests that the gradual relaxation of the strain from substrate lattice constant to an artificial lattice constant using a step grade provides two interfaces at which misfit dislocations may form. The increase in the number of strained interfaces and decrease in local strain at a particular interface where relaxation takes place reduces the number of misfit dislocations generated at each interface, thereby reducing the generation of threading dislocation. Furthermore, as misfit dislocation interaction is reduced, a more complete relaxation of the lattice constant may occur.

Surface morphology was examined for all layers using a Nomarski-interference-equipped optical microscope. Structures employing both superlattices and GaAs spacer layers were observed to have a better surface morphology with, qualitatively, less raised cross-hatching than those without superlattices and spacer

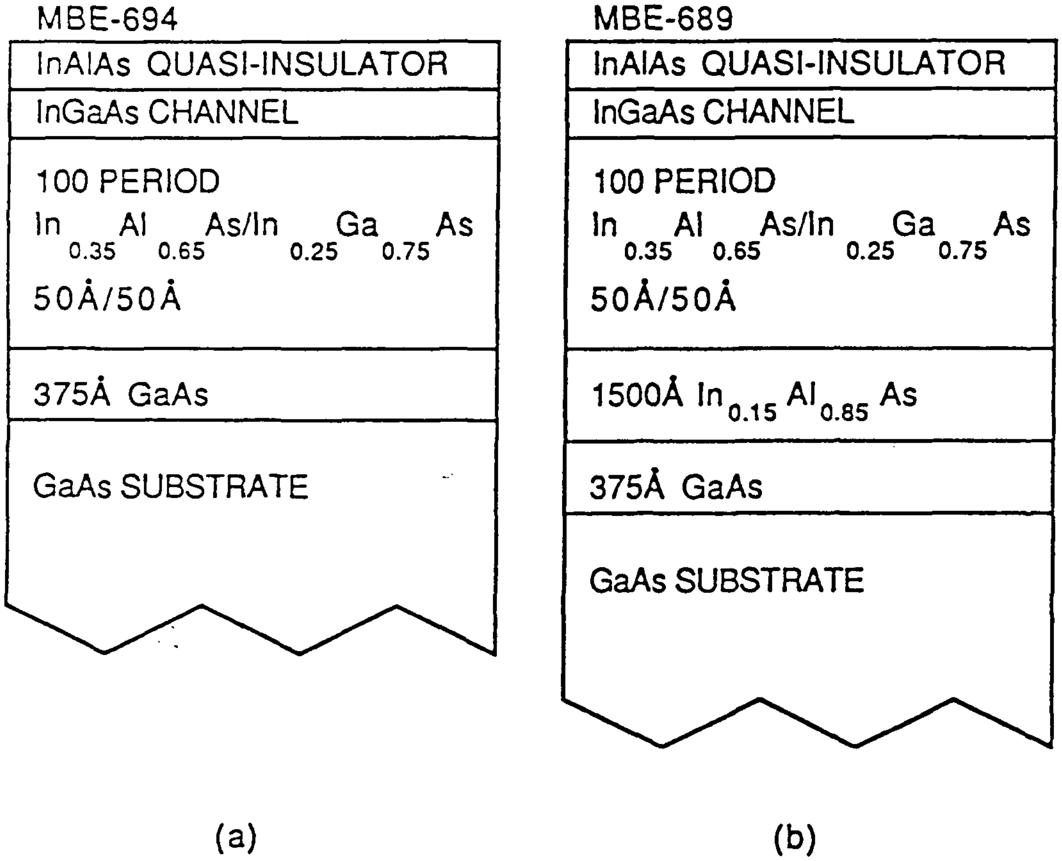

MBE-694
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
100 PERIOD
In 0.35 Al 0.65 As/In 0.25 Ga 0.75 As
50Å/50Å
375Å GaAs
GaAs SUBSTRATE
(a)
MBE-689
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
100 PERIOD
In 0.35 Al 0.65 As/In 0.25 Ga 0.75 As
50Å/50Å
1500Å In 0.15 Al 0.85 As
375Å GaAs
GaAs SUBSTRATE
(b)

Figure 4.15: Schematic cross-section of two samples utilizing $In_{0.30}Ga_{0.70}As$ equivalent buffers. (a) Sample MBE-694. (b) Sample MBE-689, which differs from sample MBE-694 by the addition of a single discrete step grade.

layers. Such cross-hatching is a result of the propagation of misfit dislocations in the layers. No structure, however, was devoid of cross-hatching.

The structures presented in this section rely on the growth of a buffer whose

TABLE 4.2: Results compiled from conductivity and Hall measurements, and the extrinsic transconductance as determined from the I-V characteristics of HIGFETs fabricated from the structures shown in Fig. 4.15. HIGFETs have L_g=5μm, W_g=280μm, and L_{sd}=16μm.

Sample	Buffer	n (cm^{-3})	μ (cm^2/V-s)	g_m (mS/mm)
MBE-694	without step	1.5×10^{17}	3760	8
MBE-689	with step grade	1.5×10^{17}	3320	27

lattice constant is equivalent to that of unstrained $In_{0.30}Ga_{0.70}As$ such that non-pseudomorphic unstrained $In_{0.30}Ga_{0.70}As$ and $In_{0.30}Al_{0.70}As$ may be grown on a GaAs substrate. Superlattices have been employed to alter the apparent lattice constant of the active device layers while providing isolation and reducing the density of dislocations propagating up to the active layers caused by the large lattice-mismatch. Thin GaAs spacer layers have been used to enhance the interface quality of InGaAs and InAlAs layers grown at 530°C. While successful transistor operation has been observed, further refinements are necessary to improve the transistor characteristics.

An $In_{0.15}Ga_{0.85}As$ Equivalent Buffer

A buffer constructed of material whose lattice constant is equivalent to that of unstrained $In_{0.15}Ga_{0.85}As$ has been designed to support a pseudomorphic channel layer made of $In_{0.30}Ga_{0.70}As$. These HIGFET structures were grown on undoped semi-insulating GaAs substrates by MBE. Details of the growth and device characteristics of the HIGFET are described in Chapter 5. All structures included a pseudomorphic Si-doped n-type $In_{0.30}Ga_{0.70}As$ channel, an undoped $In_{0.15}Al_{0.85}As$ quasi-insulating cap layer, and a buffer structure which will be discussed in detail next. These structures were evaluated electrically by means of conductivity and Hall measurements and by examining the I-V characteristics of HIGFETs processed from these layers.

Various buffer structures were investigated. All buffers consisted first of an epitaxially deposited undoped GaAs layer next to the GaAs substrate. The most superior device results were observed using the structure illustrated in Fig. 4.16. The extrinsic transconductance for 2μm HIGFETs made from these layers has exceeded 140mS/mm. This buffer utilizes a 4000Å $In_{0.15}Ga_{0.85}As$ layer adjacent to the GaAs layer/substrate, followed by a 40 period 50Å $In_{0.30}Ga_{0.70}As$- 50Å GaAs SLS, and finally another 4000Å $In_{0.15}Ga_{0.85}As$ layer just beneath the active device region. It is expected that the generation of dislocations will take place at the GaAs substrate/$In_{0.15}Ga_{0.85}As$ layer interface. The SLS is designed to act as a dislocation filter. It has an average lattice constant equal to unstrained $In_{0.15}Ga_{0.85}As$ and should not generate dislocations. The individual layers comprising the SLS, i.e. the $In_{0.30}Ga_{0.70}As$ or GaAs, are pseudomorphic with respect to one another as well as to the average lattice constant. The upper 4000Å $In_{0.15}Ga_{0.85}As$ layer acts as a final stabilizing layer for the buffer structure.

This buffer structure has been compared with another in which the SLS has been replaced by an $In_{0.15}Ga_{0.85}As$ layer of equivalent thickness. This effectively removes the SLS which is supposed to be acting as a dislocation filter. A comparison of the observed electrical parameters of devices fabricated from these layers shows superior transistor characteristics in devices which use a SLS in the buffer structure.

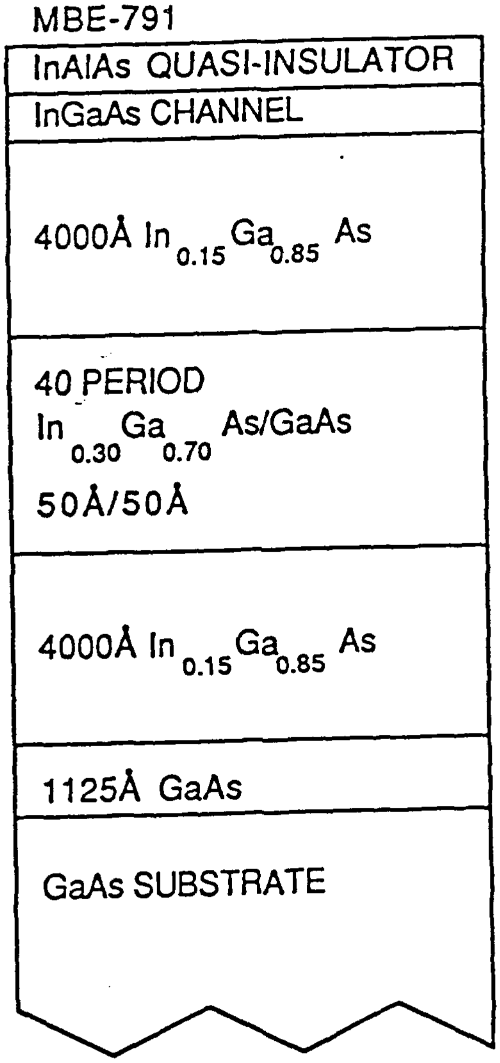

MBE-791
InAlAs QUASI-INSULATOR
InGaAs CHANNEL
4000Å $In_{0.15}Ga_{0.85}As$
40 PERIOD
$In_{0.30}Ga_{0.70}As$/GaAs
50Å/50Å
4000Å $In_{0.15}Ga_{0.85}As$
1125Å GaAs
GaAs SUBSTRATE

Figure 4.16: *Schematic cross-section* of MBE-791 which utilizes an $In_{0.15}Ga_{0.85}As$ equivalent buffer.

Conductivity and Hall measurements made on Van der Pauw configured devices fabricated from these layers show mobilities nearing 2000 cm^2/V-s with a carrier concentration greater than $3x10^{18}$ cm^{-3}. Transmission electron microscopy (TEM) has been used to evaluate the dislocation filtering properties of the buffer structures. The TEM work was done at UCSD using a Philips CM-30 Transmission Electron Microscope. An accelerating potential of 300KV is used. All samples are displayed using a two beam condition for highest contrast and samples are tilted with a g-vector=(004). (Sample preparation and TEM micrographs are the courtesy of Jessica C. P. Chang). Figures 4.17 and 4.18 compares the TEM cross-sectional views of both structure types; it suggests better confinement of the dislocations in the buffer of the sample utilizing a SLS as a dislocation filter.

The $In_{0.15}Ga_{0.85}As$ equivalent buffer described here has several advantages compared to the $In_{0.30}Ga_{0.70}As$ equivalent buffer described in the previous section. A fundamental advantage of the former is the much smaller lattice mismatch present relative to the substrate. The smaller lattice-mismatch reduces the overall relaxation required of the buffer in order to shift the lattice constant from that of GaAs to the new, artificial lattice constant, which, in this case, is equivalent to unstrained $In_{0.15}Ga_{0.85}As$. A reduction in the required degree of relaxation means a reduction in the total number of dislocations which must be formed in order to complete that relaxation. A smaller density of dislocations will mean a reduction in dislocation multiplication and interaction, and therefore, fewer propagating threading dislocations which must be filtered out. The tradeoff is a pseudomorphic $In_{0.30}Ga_{0.70}As$ channel layer. While the $In_{0.30}Ga_{0.70}As$ equivalent buffer results in an unstrained $In_{0.30}Ga_{0.70}As$ channel layer, the $In_{0.15}Ga_{0.85}As$ equivalent buffer results in a compressively strained $In_{0.30}Ga_{0.70}As$ channel layer. This strain will alter the electrical properties of the $In_{0.30}Ga_{0.70}As$ channel layer. Since the strain is compressive, the properties of the $In_{0.30}Ga_{0.70}As$

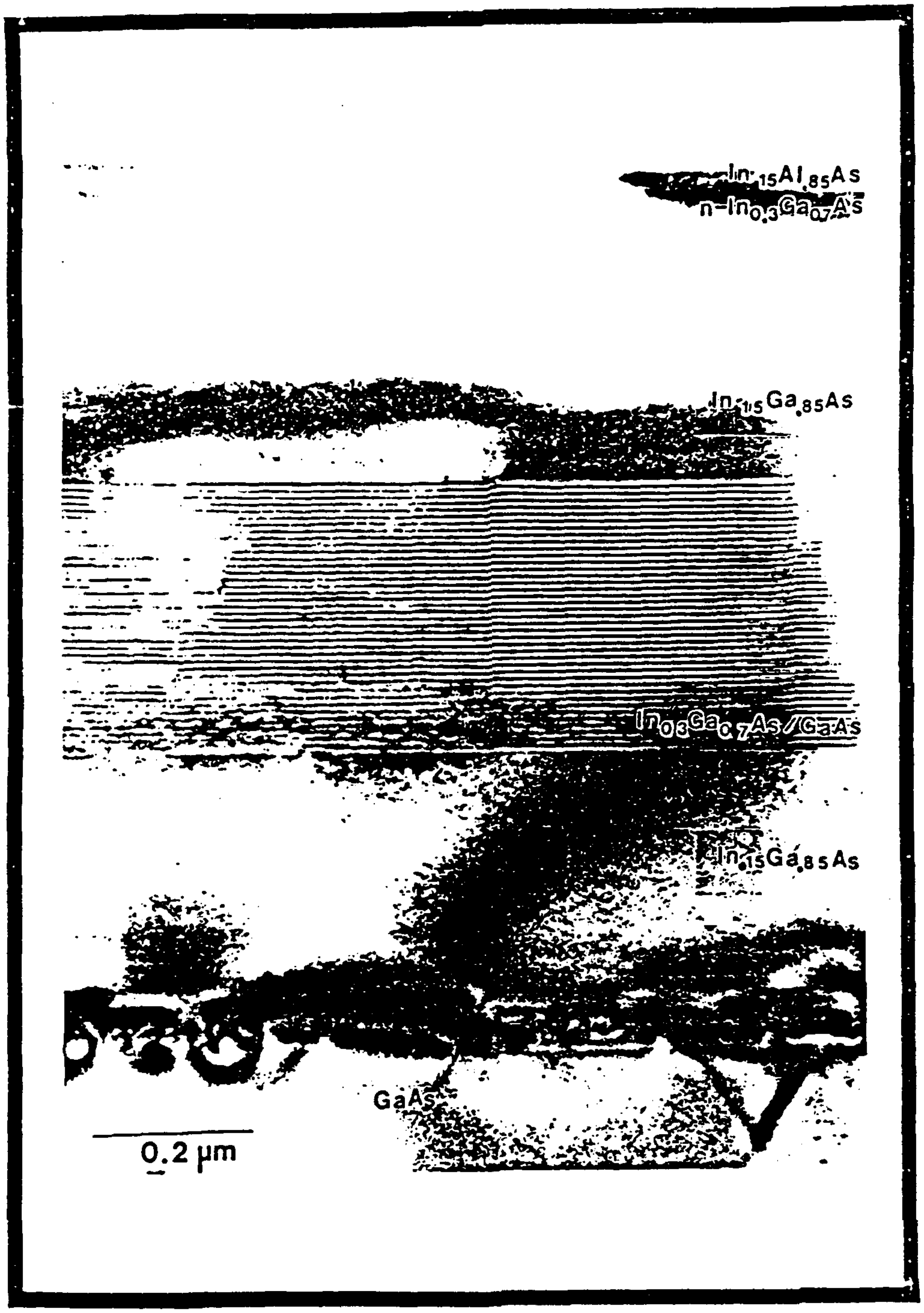

In.15Al.85As
n-In0.3Ga0.7As
In.15Ga.85As
In0.3Ga0.7As/GaAs
In.15Ga.85As
GaAs
0.2 µm

Figure 4.17: Cross-sectional transmission electron micrograph of a sample utilizing an $In_{0.30}Ga_{0.70}As$/ GaAs SLS in the buffer.

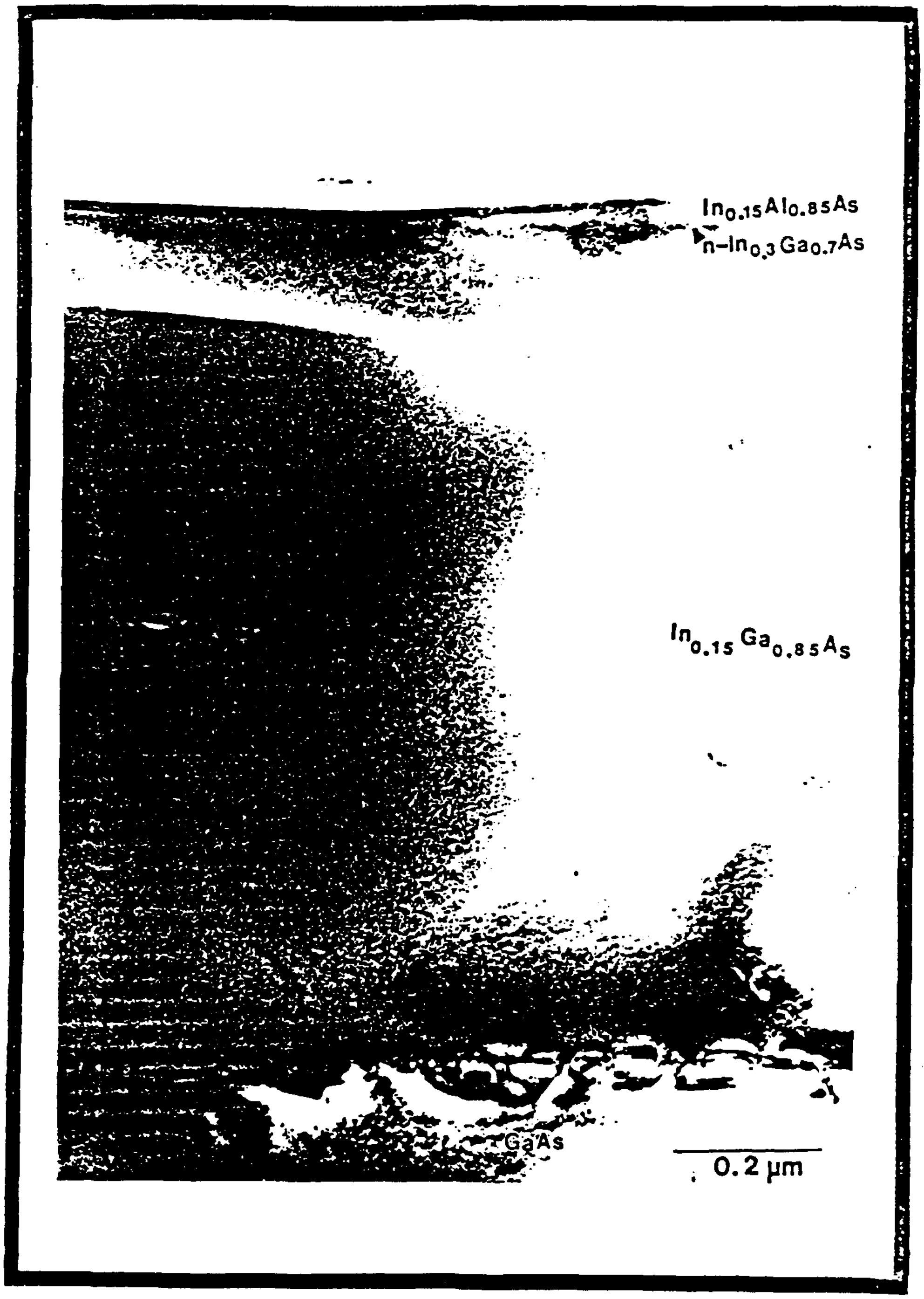

$In_{0.15}Al_{0.85}As$
$n-In_{0.3}Ga_{0.7}As$
$In_{0.15}Ga_{0.85}As$
GaAs
0.2 µm

Figure 4.18: Cross-sectional transmission electron micrograph of a sample utilizing an $In_{0.15}Ga_{0.85}As$ layer of equivalent thickness in place of a SLS in the buffer.

channel layer will be similar to a channel having a smaller In content. Thus the advantage in device performance expected from increasing the fractional indium concentration in the InGaAs channel is reduced.

Another advantage of the $In_{0.15}Ga_{0.85}As$ equivalent buffer, with respect to the $In_{0.30}Ga_{0.70}As$ equivalent buffer, is the absence of $In_xAl_{1-x}As$ layers in its buffer structure. The $In_{0.15}Ga_{0.85}As$ equivalent buffer utilizes thick InGaAs layers and a InGaAs/GaAs SLS thus avoiding the use of $In_xAl_{1-x}As$ whose growth properties under conditions used herewith are characterized by poor surface morphology and rough interfaces. By eliminating the InAlAs layers, no GaAs spacers are required to enhance the interface properties between various layers. Instead, a two minute interruption in the growth sequence under an As flux is used to allow the surface to redistribute and smooth itself prior to the growth of the next layer. These interruptions are used at three important interfaces: a) just after the SLS is grown, prior to the upper thick $In_{0.15}Ga_{0.85}As$ stabilizing layer of the buffer; b) between the buffer and channel layer; and c) after the channel is grown, prior to the growth of the undoped quasi-insulating $In_{0.15}Al_{0.85}As$ layer.

As has been discussed in Section 4.5.1, a continuous linearly graded layer with overshoot in the buffer structure may be employed to improve relaxation of the lattice constant prior to the growth of the SLS. Such a structure was grown and evaluated. A composition versus depth profile of this device is shown in Fig. 4.19. Results show this device to be as good as the best obtained thus far for structures using an $In_{0.15}Ga_{0.85}As$ equivalent buffer. Analysis of this structure using X-ray diffractometry is hampered by a slurring of the peaks in the rocking curve data due to the linear graded region of the buffer. This inhibits a comparison of the degree of relaxation between samples with and without a linearly graded layer with overshoot in the buffer structure.

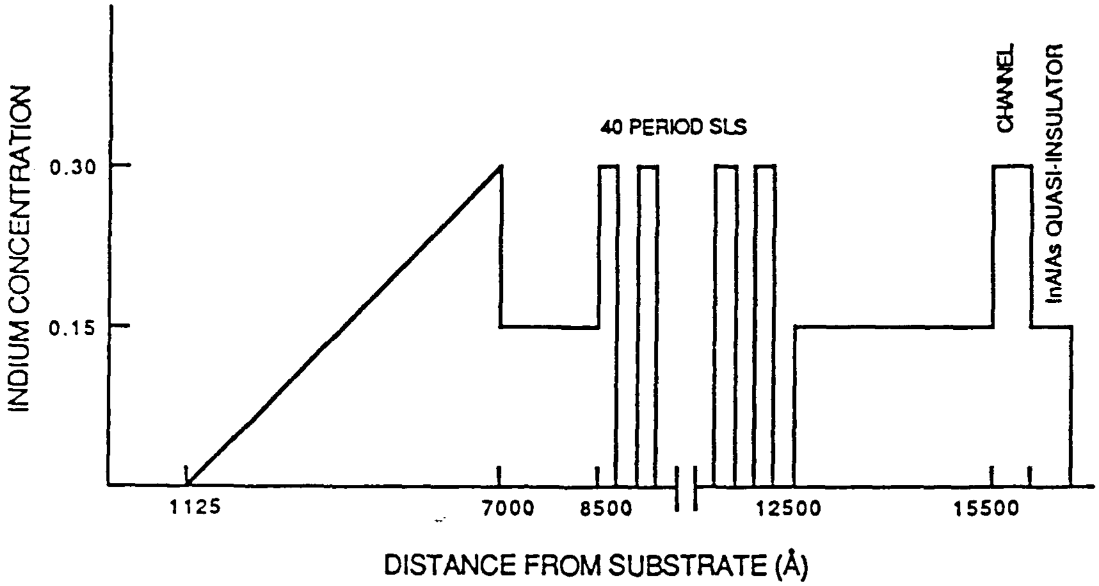


Figure 4.19: Composition versus depth profile of a sample grown in which a linearly graded layer with overshoot is utilized in the buffer. The sample uses $In_xGa_{1-x}As$/ GaAs layers to form an $In_{0.15}Ga_{0.85}As$ equivalent buffer.

Buffer Analysis using X-ray Diffractometry and RHEED

X-ray diffractometry was used to examine the degree of relaxation in the buffer structure and the composition of various layers. X-ray diffraction is a powerful non-destructive means for determining lattice-mismatch or compositions in multi-layered heterostructures. The Philips PW-1729 double crystal X-ray apparatus at UCSD utilizes a Bartels 4-crystal monochromator to deliver highly collimated monochromatic radiation. The Bartels 4-crystal monochromator is composed of two U-shaped single-crystal blocks of dislocation-free germanium oriented for diffraction at the (440) planes.

The use of such a monochromator allows high resolution diffractometry which is important when examining heterostructures composed of thin epitaxial layers.

X-ray measurements were compared with the compositions as determined from RHEED intensity oscillation measurements. $In_{0.15}Ga_{0.85}As$ equivalent buffer structures composed of a SLS and thick $In_{0.15}Ga_{0.85}As$ layers have been analyzed by double crystal x-ray diffractometry to reveal the degree of relaxation in the buffer structure and determine the true artificial lattice constant induced by this non-pseudomorphic buffer. The importance in determining the artificial lattice constant is underlined by the necessity to insure the pseudomorphic nature of the channel which is grown subsequently on that buffer. X-ray rocking curves are dominated by peaks belonging to the GaAs substrate, the $In_{0.15}Ga_{0.85}As$ layers, and the SLS. An example of a typical x-ray rocking curve is shown in Fig. 4.20. This curve corresponds to the structure shown earlier in Fig. 4.16. Figure 4.20 is characterized by five major peaks which will be designated peaks A through E starting from the left-most peak in the figure and moving towards the right. Thus, the very sharp peak of greatest intensity and narrowest width is peak D. Peak D is the peak corresponding to the GaAs substrate. Immediately to peak D's left is peak C which corresponds to the $In_{0.15}Ga_{0.85}As$ layers and the center or primary peak of the superlattice. The remaining peaks, including the slight shoulder on peak D, are related to the superlattice structure. While Peak E is not apparent from the X-ray data of Fig. 4.20, higher detailed X-ray scans reveal a well established SLS-related peak immediately to the right of peak D. Since the SLS is situated in the center of the buffer structure, it may be used as a reference for determining the relaxation in the buffer structure. A periodic structure such as a superlattice will be reflected in the x-ray rocking curve data by a primary peak and several other periodic peaks, referred to as satellite peaks. The primary peak will correspond to the average lattice constant of the SLS as a whole. The superlattice periodicity, Λ, may be given as

$$\Lambda = N_w a_w + N_b a_b = d_w + d_b \,, \tag{4.2}$$

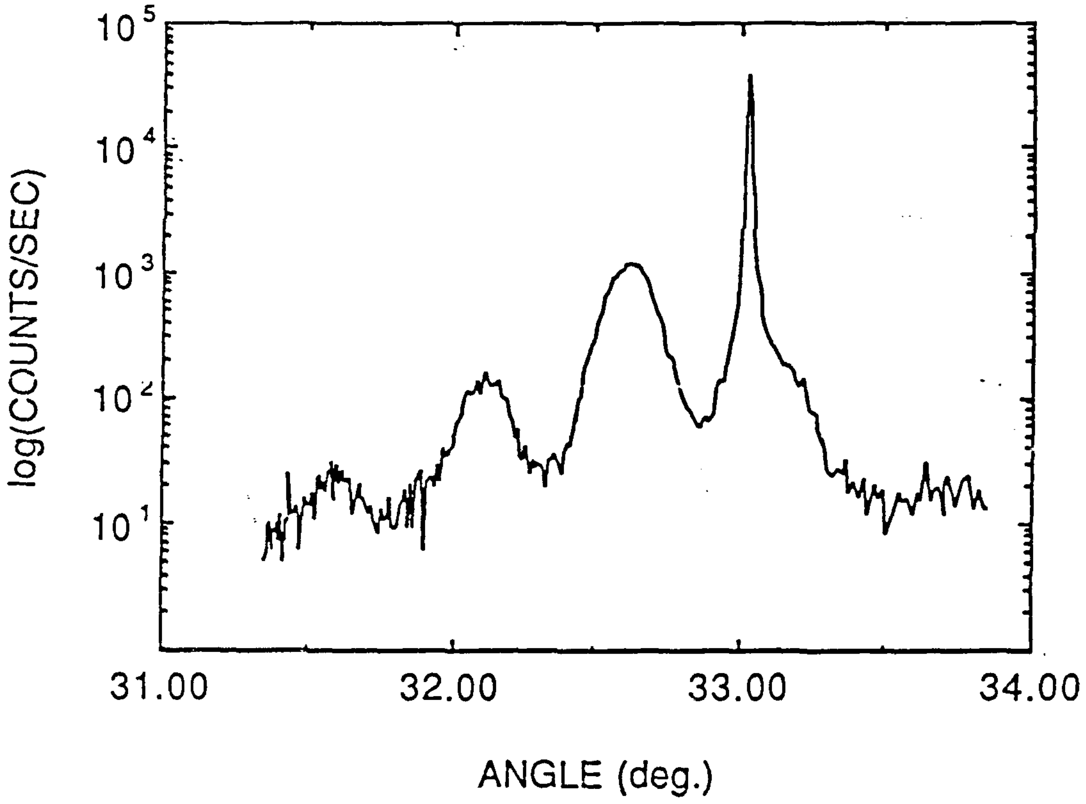


Figure 4.20: Double-crystal X-ray profile as obtained for a sample having a structure equivalent to sample MBE-791. The rocking curve is dominated by peaks corresponding to the GaAs substrate, the $In_{0.15}Ga_{0.85}As$ layers, and the $In_{0.30}Ga_{0.70}As$/ GaAs SLS.

where N_w and N_b are the number of monolayers in a well and barrier, respectively, a_w and a_b are the well and barrier monolayer spacings, respectively, and d_w and d_b are the thicknesses of the well and barrier, respectively. The condition for satellite peak occurrence is

$$\frac{2\sin\theta_n - 2\sin\theta_{SL}}{\lambda} = \pm\frac{n}{\Lambda}, \tag{4.3}$$

where n is the order peak number, θ_n is the angle of the nth order peak, is the angle of the 0th order peak, and λ is the wavelength. Standard notation dictates that positive higher order peaks correspond to satellite peaks at larger angles than the 0th order peak and, conversely, negative higher order peaks correspond to satellite peaks at smaller angles than the 0th order peak. For the Philips PW-1729 double crystal X-ray apparatus at UCSD, the wavelength corresponds to the Cu $K\alpha_1$ value, λ=1.5405Å. The relaxation of the buffer structure will cause a broadening in the observed X-ray peaks corresponding to layers closest to the substrate/buffer interface which are under the greatest stress and therefore will experience the greatest relaxation. This will affect the linewidth of the peak (peak C in Fig. 4.20) corresponding to the $In_{0.15}Ga_{0.85}As$ layer immediately adjacent to the substrate. Since the 0th order peak of the SLS and peak corresponding to the upper $In_{0.15}Ga_{0.85}As$ layer are superimposed at approximately the same angle as the peak corresponding to the $In_{0.15}Ga_{0.85}As$ layer which is immediately adjacent to the substrate, it is necessary to apply the information which may be obtained from analyzing the satellite peak information of the SLS to determine the SLS average lattice constant. The condition for satellite peak occurrence may be used to predict the correct location of the center or 0th-order peak of the SLS. Once the angle is determined, Bragg's law, given as

$$m\lambda = 2d\sin\theta, \tag{4.4}$$

where m is the reflection order and d is the spacing between atomic planes, may be applied. For the x-ray apparatus at UCSD, m=4. Since the layers of greatest concern are assumed to have undergone relaxation, no correction for tetragonal distortion is necessary and Vegard's law may be applied directly to determine the composition. An example is shown in Table 4.3. This sample has a structure identical to that illustrated in Fig. 4.16. Included in this table are results obtained from RHEED intensity

Table 4.3: Summary of observed and calculated angles obtained from the x-ray diffraction measurement shown in Fig. 4.20. and the resulting In mole fractions as determined from double crystal x-ray diffraction and RHEED intensity oscillation analysis for the average SLS composition.

X-ray results

	nth-order peak				
	-2	-1	0	+2	calculated 0
observed angle	31.635°	32.130°	32.664°	33.635°	32.630°

Average SLS composition

	goal	uncorrected 0th-order peak	corrected 0th-order peak	RHEED
In mole fraction	0.1500	0.1365	0.1496	0.157

oscillation measurements. RHEED intensity oscillation measurements were made prior to the growth of any structure in order to determine the compositions and thicknesses to be used. RHEED intensity oscillations have been discussed in Chapter 2. Using the assumptions presented above, the layers grown above the SLS are assumed to have undergone complete strain relaxation. Discrepancies between the two measurements may be attributed to errors in the measurement techniques and incomplete relaxation of the buffer structure. Although equilibrium theory predicts that the thickness of the buffer structure should dictate a complete relaxation since the critical thickness has been exceeded for the misfit present at the substrate/ buffer interface, partial elastic and plastic deformation may coexist resulting in an incomplete relaxation of the structure.

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Strained-layer Heterojunction Insulated-gate Field Effect Transistors

Introduction: Design Considerations

In the preceding chapters, the growth of strained-layer structures has been discussed. Chapter 2 illustrated the importance of MBE growth of various III-V compounds and discussed some of their associated properties. Chapter 3 discussed strained material systems providing insight to the complications of lattice-mismatched systems. Chapter 4 illustrated the application of dislocation filtering and strain relaxation which may be applied to fashion new, high-quality, strained-layer devices. In this chapter the details for the application of heteroepitaxial layers for prototype devices is discussed. A heterojunction insulated gate field effect transistor (HIGFET) is described which will demonstrate the inherent and potential advantages of strained layer systems.

The HIGFET employs a highly doped thin conducting channel which is separated from the gate metal by an undoped, totally depleted wide-bandgap semiconducting layer used as a quasi-insulator. Such a structure has been described in the literature as a heterojunction insulated-gate, insulator-like gate, insulator-assisted gate, heterostructure gate, Schottky-enhanced gate, an MIS-type or MIS-like or simply an MIS gate. Despite the colorful nomenclature, this type of structure is considered here to be a member of the insulated gate structures such that its interaction with external fields can be treated under the same boundary conditions as those applied to metal-oxide-silicon (MOS) or metal-insulator-semiconductor (MIS) structures. The HIGFET emulates the configurational simplicity of the MOSFET while taking full advantage of the more favorable charge carrier transport properties of the III-V semiconducting compounds.

Ideally, the MIS structure may be considered as either a linear or non-linear parallel plate capacitor in which the insulator is considered principally in terms of its dielectric behavior. An electric potential may be applied between the metal and semiconductor producing an electric displacement vector which is perpendicular to the surface and is continuous across the metal-dielectric and dielectric-semiconductor interfaces. The electric field in the semiconductor is directly related to the electric field in the insulator. Thus, as the charge applied to the metal gate is varied, the mobile charge of opposite sign in the semiconductor is varied. In realistic cases, the electric displacement vector is discontinuous across the dielectric-semiconductor interface. This is the result of trapped charges at the insulator-semiconductor interface. These trapped charges may be the result of defects or impurities localized at the interface, discontinuities in the lattice at the interface, or perturbations in the electron states which are near the semiconductor surface. These trapped charges must be minimized in order to obtain acceptable operating characteristics in the transistor.

While the Si-SiO_2 system has near ideal properties for an semiconductor-insulator system, a major stumbling block for III-V semiconductors has been the lack of a suitable gate insulator. Synthetic heteromorphic or homomorphic insulators on III-V semiconductor surfaces have always produced a high density of extrinsic acceptor-like and/or donor-like surface states which cause severe surface depletion or accumulation of the channel and may even pin the channel Fermi level. The presence of these surface or interface states may produce long term drift of the gate voltage which is required to set the surface charge density at flat band in MIS structures. Furthermore the spatial and energy distributions of bulk traps in the insulator have been related to a logarithmic dependence of the DC transistor parameters with time. These problems are absent in devices which use a semiconductor as a quasi-insulator. While amorphous deposited or grown insulators may produce interface state densities in excess of $10^{12}cm^{-2}$, the interface state density in the $Al_{1-x}Ga_xAs/GaAs$ system is on the order of $10^{10}cm^{-2}$, while that of the $In_xAl_{1-x}As/InP$ system[1], even if lattice-mismatched, is only $10^{11}cm^{-2}$. This suggests that a suitable HIGFET technology may be found provided the selection of the semiconductor quasi-insulator is chosen to have the necessary attributes of a conventional insulator. Therefore, the III-V semiconductor which is chosen to be the quasi-insulator must provide adequate isolation between the metal gate and the conducting channel. It must have a dielectric constant which is dispersionless at low frequencies. It must have a low interface state density, a negligibly small fixed charge, and a low bulk trap density. It should have a large breakdown strength to allow a large operating range for applied gate voltages. The breakdown strength will be directly associated with the defect density in the material since these defects may act as nucleation sites for impact ionization. It should have a reasonably large barrier height with an adjusted thickness to prevent tunneling and thermally-assisted tunneling over the barrier. The quasi-insulator should also have a sufficiently large bandgap so that at room temperature its electron density is negligible. Its thickness must be considerably less than its effective depletion depth to insure that the layer is fully depleted. Since the quasi-insulator must sustain only a displacement current and not a conduction current, its conduction bandedge offset, ΔE_c, at the quasi-insulator/channel interface should be as large as possible.

For high performance, high frequency HIGFETs the channel must have a high electron mobility, large peak and saturation electron velocity, and, to prevent intervalley electron transfer, large energy separations between the intra-conduction band valleys. The thickness and doping density must be chosen with regard to the mode of operation of the HIGFET; i.e. depletion or enhancement mode. The doping density will determine the free electron concentration, the pinch-off voltage, and the transconductance. For devices which require a large dynamic range the doping concentration for a given bandgap must not be so large that it will cause impact ionization of electrons in the channel.

Since lattice defects will affect the material parameters of the channel, the density of these defects, both intrinsic and extrinsic, must be minimized. To prevent defects which originate outside the channel layer requires careful consideration of the buffer layers which act as the foundation for the active region of the device. Several of these considerations have been developed in Chapter 4. Careful use of grading and strained layer structures such as superlattices, can prevent the propagation of defects formed at the buffer/substrate interface from reaching the active regions of the device. Furthermore, the buffer layer can be used to create a pseudo-substrate which has an artificial lattice constant differing from the original substrate.

The InAlAs/InGaAs HIGFET

Introduction

Figure 5.1 shows the InAlAs/InGaAs material system plotted as lattice constant versus energy. For every composition of the ternary alloy $In_xGa_{1-x}As$ there exists a corresponding ternary alloy of $In_yAl_{1-y}As$ with an identical lattice constant. $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$, which may be grown lattice matched to one another and to InP, are among the most investigated compositions. While the InGaAs alloy has a direct bandgap over its entire compositional range, the InAlAs alloy has a direct bandgap over a limited compositional range becoming indirect for high Al concentrations. A plot of the energy versus composition for the $In_yAl_{1-y}As$ ternary

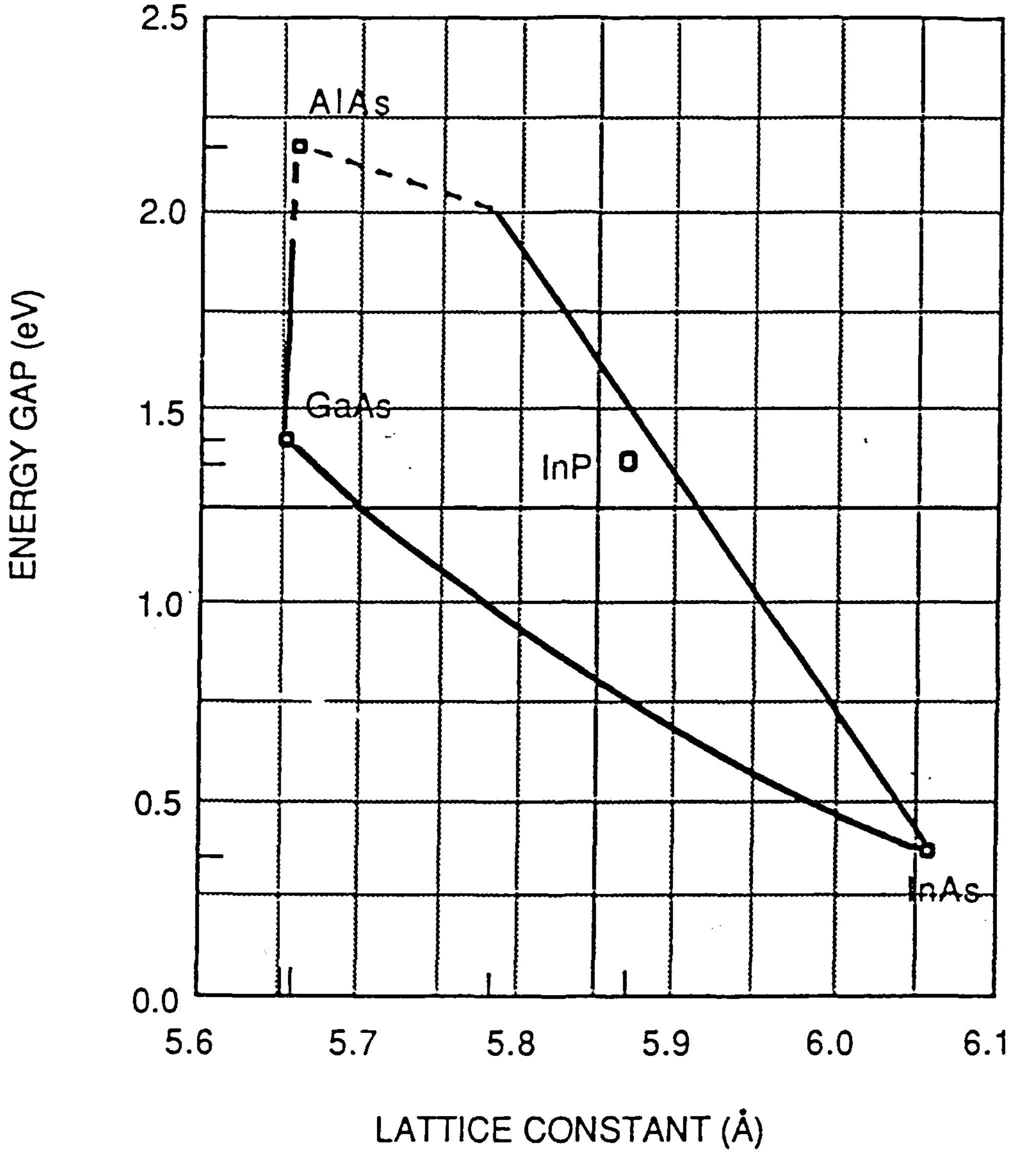

Figure 5.1: Variation in the room temperature energy gap with the lattice constant for the ternary alloys InAlAs and InGaAs.

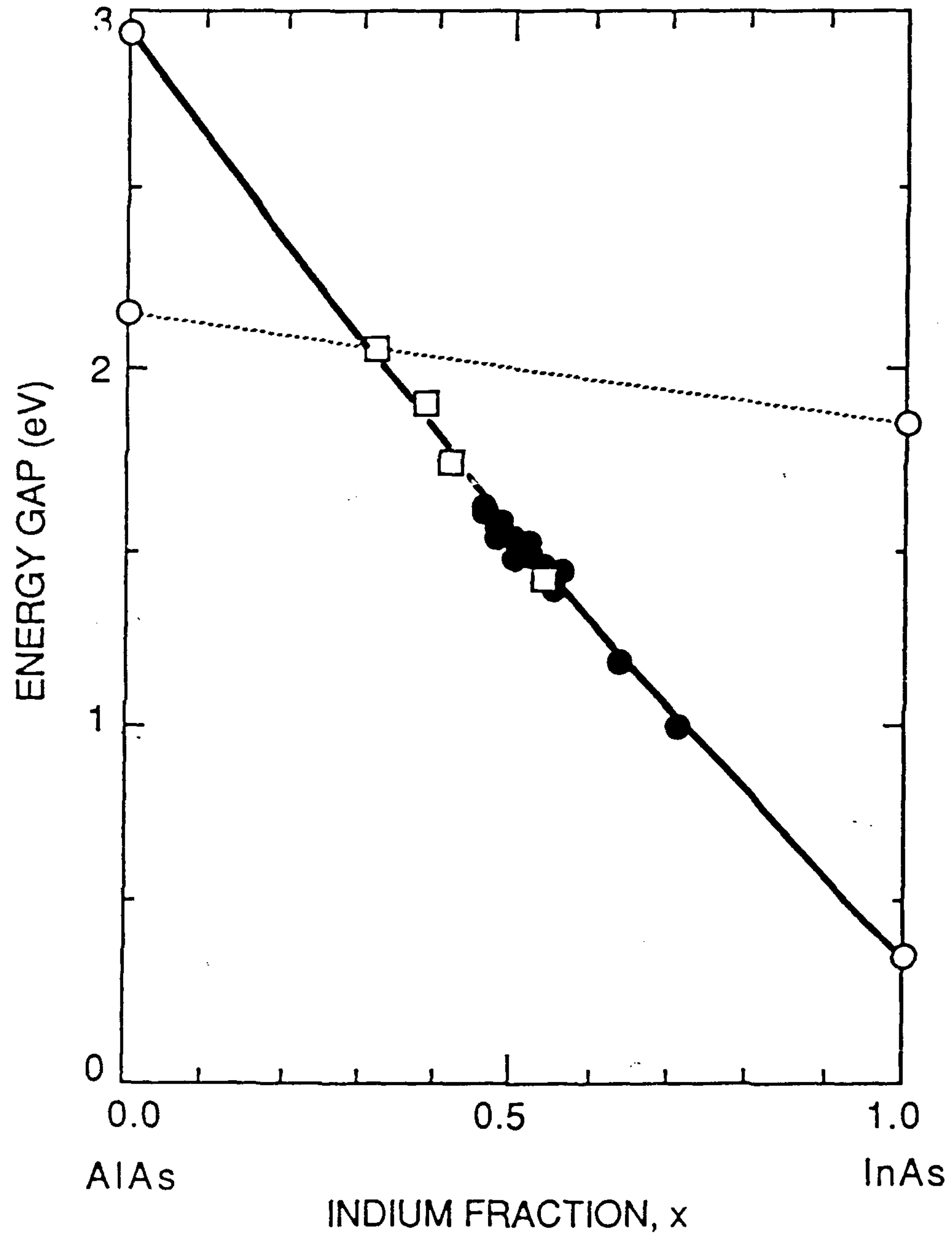

Figure 5.2: Variation in the room temperature energy gap of $In_xAl_{1-x}As$ showing both Γ (solid line) and X (dotted line) bands. Solid circles show data determined by the author using photoluminescence and X-ray measurements. Open squares show data from Lorenz and Onton using cathodoluminescence measurements.

alloy is shown in Figure 5.2.[2]

Pseudomorphic $In_xGa_{1-x}As$ channel layers may be grown on GaAs substrates provided they do not exceed a critical thickness governed by the lattice mismatch between these two materials. As the InAs molar fraction of the $In_xGa_{1-x}As$ layer is increased the critical thickness is decreased. To overcome the limitation imposed by the critical thickness without varying the $In_xGa_{1-x}As$ channel composition, a buffer layer may be interposed between the channel and GaAs substrate which shifts the substrate lattice constant to a new artificial lattice constant. The resulting shift can reduce or eliminate the lattice mismatch of the channel layer. Superposed on the channel layer, $In_yAl_{1-y}As$ layers may be grown which are lattice matched to the new artificial lattice constant of the buffer and may be grown without the penalty imposed by strain-dependent parameters.

The HIGFET utilizes a metal-insulator-semiconductor type gate configuration. An aluminum gate metal is placed directly on the InAlAs cap layer, which behaves as a quasi-insulator, and is in turn adjacent to the n^+-InGaAs channel. A balance between the material advantages and material constraints will govern the design of the HIGFET. The HIGFET design may be divided into three areas of interest, the channel, the buffer, and the quasi-insulator. Each of these is described below.

The Channel

The channel has a composition of $In_{0.30}Ga_{0.70}As$. Once the channel composition is chosen the device is designed to accommodate this layer. As the In concentration of the $In_xGa_{1-x}As$ channel is increased it is expected that the electron effective mass will decrease and the Γ-L intervalley energy difference will increase compared to GaAs. The total change in these parameters is dependent on the strain present in the $In_xGa_{1-x}As$ channel layer. If the channel is grown unstrained and lattice-matched to a new artificial lattice constant created by the buffer then no correction is necessary in determining the band structure parameters. However, if the channel layer is grown pseudomorphically with respect to the buffer layer and the artificial lattice constant established by the buffer layer than the strain-dependence of the parameters must be taken into account. In this chapter emphasis will be on pseudomorphic $In_xGa_{1-x}As$ channel HIGFETs.

The channel layer must be doped in order to supply the necessary carriers for transport. $In_xGa_{1-x}As$ layers were doped with Si during growth in the MBE reactor using a precalibrated Si molecular flux density. Layers were doped to provide an electron concentration, $n \geq 2 \times 10^{18}$ cm^{-3}. Good current linearity in the HIGFET is expected for these electron densities. Because of the high doping concentration, the electron mobility and velocity is expected to be dominated by impurity scattering. The channel thickness is chosen to be very thin, $a \leq 180$Å. Although such layers might constitute degenerately doped quantum wells the subsequent analysis of their properties will be treated in the classical approximation. Since the channel thickness is small with respect to the gate length, the resulting high aspect ratio suggests that short-channel effects in the HIGFET will not be a problem. The desirability of a thin channel is fortuitous since the growth of elastically strained materials is governed by thickness limitations. The critical thickness criteria of the channel will determine the necessary artificial lattice constant of the buffer. If the channel thickness is chosen to be at most 180Å and the critical thickness of this layer is chosen to be the same value, then the corresponding lattice-mismatch needed to equate the thicknesses requires that the $In_{0.30}Ga_{0.70}As$ channel reside on a buffer whose average artificial lattice constant is equivalent to that of $In_{0.15}Ga_{0.85}As$. For a pseudomorphic $In_{0.30}Ga_{0.70}As$ channel grown on a buffer of $In_{0.15}Ga_{0.85}As$, the strain corrected bandgap of the $In_{0.30}Ga_{0.70}As$ channel is E_g=1.071eV.

The Buffer

Among the many considerations in designing field effect transistors is the desire to have high carrier mobility and high saturation velocities in the conducting channel. This requires lattice defects and other cystalline imperfections which would induce scattering in the channel to be at a minimum. In chapter 4, consideration is given to the growth of buffer layers between the channel and substrates of FETs. The purposes of these buffers is to effect a lattice constant change, relieve strain, and confine dislocations spatially within the buffer layers for structures in which the substrate and desired channel lattice constants are *mismatched*. Two different devices were described: a buffer structure whose relaxed lattice constant is present in unstrained $In_{0.15}Ga_{0.85}As$, and one whose lattice constant is that of unstrained $In_{0.30}Ga_{0.70}As$. The $In_{0.30}Ga_{0.70}As$ channel will be elastically deformed , in compression, in the first structure and unstrained in the second structure. The emphasis in this section will be on devices utilizing a relaxed lattice constant buffer layer equivalent to unstrained $In_{0.15}Ga_{0.85}As$.

One purpose of interposing a buffer which creates an artificial lattice constant is to reduce the lattice mismatch between substrate and conducting channel in the FET. If an $In_{0.30}Ga_{0.70}As$ channel were to be grown directly on the GaAs substrate the corresponding strain would limit the effective thickness of the channel layer. A channel layer which is pseudomorphic would be too thin while a thicker layer would exceed the critical thickness and contain a high density of defects. By shifting the lattice constant to one equivalent to unstrained $In_{0.15}Ga_{0.85}As$ through the use of buffer layers, the effective stress on the channel has been reduced. From the details presented in Chapter 3, the critical thickness for a pseudomorphic $In_{0.30}Ga_{0.70}As$ layer on an $In_{0.15}Ga_{0.85}As$ substrate is about 180Å. Therefore, this provides a design guide for the maximum thickness which may be tolerated for the device channel.

If a larger InAs molar concentration in the $In_xGa_{1-x}As$ channel layer were desired, the artificial lattice constant induced by the buffer would have to be increased in order to maintain a pseudomorphic channel layer at the same thickness. Increasing the artificial lattice constant means readjusting the compositions used in the buffer structure. Attention must be paid to strain relaxation. Since the demands on the buffer is to provide an artificial lattice constant with a higher average InAs molar fraction, then the lattice mismatch between buffer and substrate is increased. Graded buffers may be employed to reduce the large lattice discontinuity and thus reduce the generation of unwanted threading dislocations. Furthermore, the average lattice constant of the SLS must be shifted in order to maintain lattice-matching throughout the buffer structure. This requires that the compositions of the individual SLS layers be altered. The individual layers must be pseudomorphic yet thick enough to insure dislocation filtering in the superlattice. That is to say, it is not enough to have a SLS; the SLS must also act as a dislocation filter. This balance of requirements and considerations must be made to properly design the buffer.

The Quasi-insulator

The objective of using a large bandgap crystalline semiconductor instead of an amorphous dielectric material in order to insulate the metal gate from the channel is to overcome the inherent disadvantages of amorphous insulators. $In_xAl_{1-x}As$ has been chosen as the quasi-insulator because of its potential advantages intended to overcome the shortfalls of non-semiconductor insulators. $In_{0.15}Al_{0.85}As$ was chosen as the quasi insulator because it may be grown closely lattice-matched to the artificial lattice constant of the buffer thus reducing strain differences within the structure which serves to reduce the potential nucleation of defects. Unstrained $In_{0.15}Al_{0.85}As$ has an indirect fundamental bandgap of E_g=2.094eV. The $In_{0.15}Al_{0.85}As$ quasi-insulator is grown directly on the tetragonally distorted $In_{0.30}Ga_{0.70}As$ channel layer. Although the channel and quasi-insulator are not lattice-matched, lattice-mismatched quasi-insulators have been used previously[3] and do not present any potentially serious problems. $In_xAl_{1-x}As$ is grown at the same substrate temperature, T_{sub}=530°C, as is the rest of the device. A major advantage of the $In_xAl_{1-x}As$ quasi-insulator is that it may be grown *in situ* in the MBE reactor as an epitaxial layer. This avoids complicated regrowth outside the MBE reactor as is the case for many conventional insulators deposited on III-V structures. Assuming that the conduction bandedge offset is related to the bandgap difference between $In_{0.15}Al_{0.85}As$ and $In_{0.30}Ga_{0.70}As$ by $\Delta E_c/\Delta E_g=0.65$, which is similar to that of the $GaAs/Al_xGa_{1-x}As$ system, it is estimated that ΔE_c=0.703 eV. This is expected to be sufficient for HIGFET applications although it is considerably smaller than the ΔE_c=3 eV of the Si/SiO_2 system. The indirect bandgap of the InAlAs may assist in the reduction of any leakage current through the quasi-insulator layer. The InGaAs channel adjacent to the quasi-insulator layer has a direct bandgap, thus a direct to indirect heterojunction exists. It is assumed that such a heterojunction will reduce the tunneling current from the channel into the InAlAs, and therefore reduce the overall current through the quasi-insulator. The $In_{0.15}Al_{0.85}As$ must be grown undoped in order to be totally depleted as well as to minimize the effects of ionized impurities which behave as fixed charges in it. A low interface state density at the quasi-insulator/channel interface is desirable to prevent Fermi-level pinning and to avoid D.C. drift of the transistor parameters. These last problems are often related to material quality which may be influenced by differences in lattice constant, phase differences, or differences in thermal expansion coefficients between channel and insulator. The quality of the $In_xAl_{1-x}As$ is largely dependent on the MBE growth parameters which must be carefully regulated to insure that the material problems are minimized and that the material is reproducible.

The static dielectric constant of $In_{0.15}Al_{0.85}As$ may be determined by interpolating between the respective parameters of the binary alloys and is calculated to be $\varepsilon=10.74$. $In_xAl_{1-x}As$ is expected to have a large Schottky barrier height for low molar fractions of In;[4] $\phi_b=1.2$ eV for $In_{0.15}Al_{0.85}As$.

It is noteworthy that the composition of the quasi-insulator may be altered in order to optimize it for specific device applications without undue penalties in HIGFET performance. Furthermore, any increase in the interface state density as a result of defects induced in the quasi-insulator by a large lattice-mismatch between the channel and quasi-insulator is expected to be moderate.[2] The InAlAs/InGaAs system allows a broad range of materials to be applied to HIGFETs and similar devices. As the channel composition is varied, the design parameters of the device remain straightforward since the quasi-insulator composition is equally variable.

Experimental Work

Prototype device structures were grown on (100)-oriented semi-insulating GaAs substrates by molecular beam epitaxy (MBE). Before introduction into the MBE reactor, all GaAs substrates were solvent degreased and then etched in a mixture of $H_2SO_4:H_2O:H_2O_2$ (5:1:1) to remove mechanical damage resulting from polishing. The substrates were mounted on molybdenum sample holders using an interfacial layer of molten In. Prior to growth, substrates were subjected to surface oxide removal by heating to about 610°C under an arsenic flux. The purpose of having an As flux impinging on the substrate surface is to prevent degradation of the substrate due to incongruent surface dissociation at the oxide desorption substrate temperature. The arsenic-stabilized surfaces were observed by RHEED and then cooled to the growth temperature of 530°C.

Growth consisted of a buffer structure, a heavily doped n^+-$In_{0.30}Ga_{0.70}As$ channel layer and an undoped $In_{0.15}Al_{0.85}As$ quasi-insulating cap layer, utilizing interrupted growth sequences at critical points. The cross-section of a typical growth sequence followed by device fabrication is illustrated in Fig. 5.3. The buffer consists of an undoped GaAs buffer layer followed by an abrupt compositional step of $In_{0.15}Ga_{0.85}As$. This step, coupled with the SLS structure, will plastically deform by generating misfit dislocations because of the lattice mismatch and layer thickness relative to the GaAs substrate. The SLS structure is designed to have an average lattice constant equivalent to that of the relaxed $In_{0.15}Ga_{0.85}As$ alloy. The SLS is composed of 40 periods of $In_{0.30}Ga_{0.70}As$/GaAs alternating layers. Each individual layer is 50Å in thickness and well below the pseudomorphic critical thickness. Growth rates are determined from RHEED intensity oscillation measurements performed prior to the growth of the HIGFET structure to insure accurate control of thicknesses. The SLS will filter out threading dislocations which are generated at and propagating from the $In_{0.15}Ga_{0.85}As$/GaAs substrate interface. The SLS is followed by a second $In_{0.15}Ga_{0.85}As$ buffer layer which acts as a stabilizer for the buffer structure. The Si-doped n^+-$In_{0.30}Ga_{0.70}As$ channel is grown next, followed by the undoped $In_{0.15}Al_{0.85}As$ quasi-insulating cap layer. Finally, a thin GaAs capping layer with a thickness on the order of 20Å is grown to protect the InAlAs quasi-insulator layer from oxidation upon exposure to the environment. Interruptions of two minute duration were

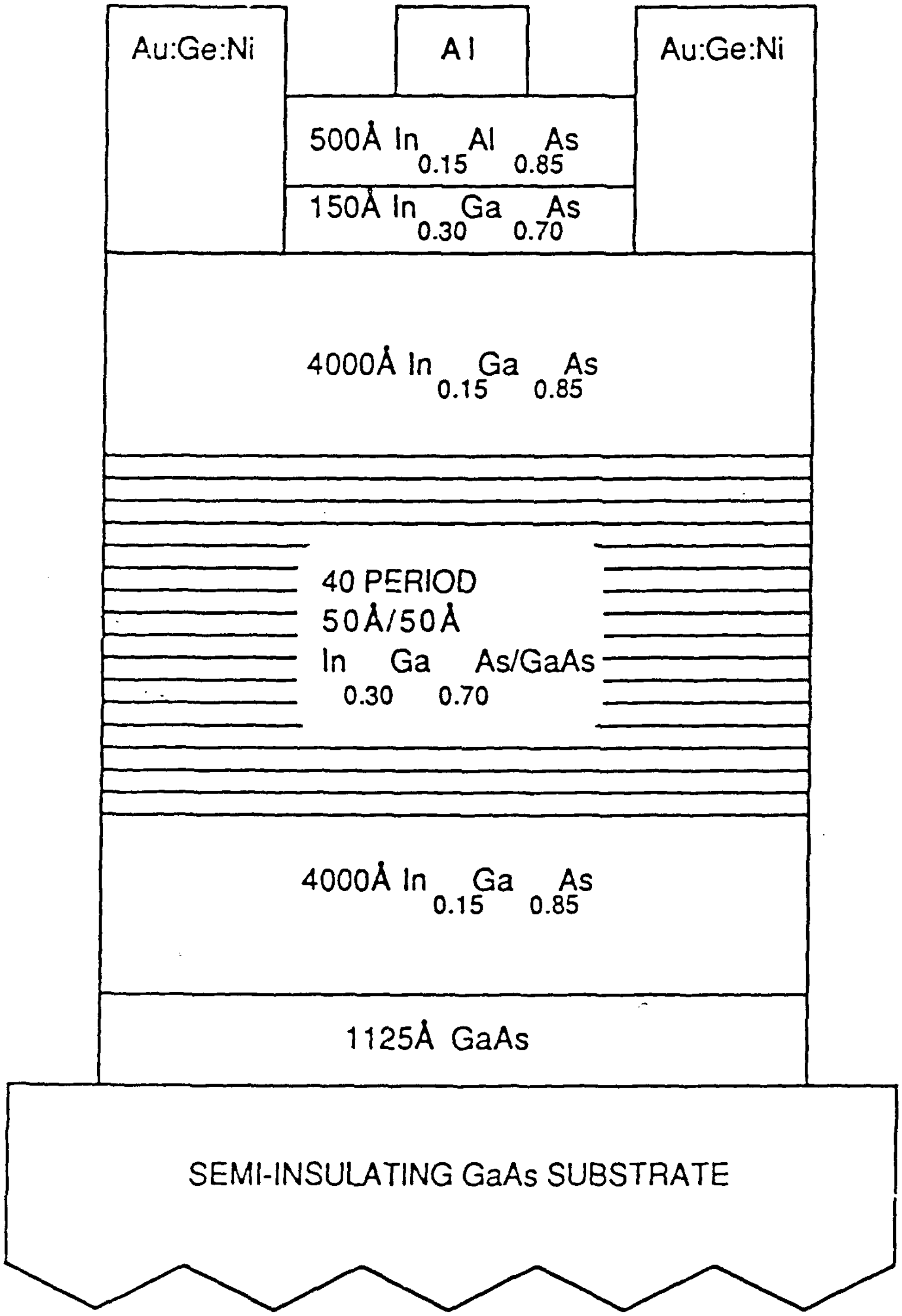
Au:Ge:Ni
Al
Au:Ge:Ni
500Å $In_{0.15}Al_{0.85}As$
150Å $In_{0.30}Ga_{0.70}As$
4000Å $In_{0.15}Ga_{0.85}As$
40 PERIOD
50Å/50Å
$In_{0.30}Ga_{0.70}As$/GaAs
4000Å $In_{0.15}Ga_{0.85}As$
1125Å GaAs
SEMI-INSULATING GaAs SUBSTRATE

Figure 5.3: Schematic cross-section of a typical InGaAs/InAlAs HIGFET structure. This structure uses a buffer whose unstrained lattice constant is equivalent to that of $In_{0.15}Ga_{0.85}As$.

employed in the growth sequence during the growth of the buffer and before and after the growth of the channel layer. The interruptions are used to aid in allowing smooth interfaces between different composition layers.[5] This is of particular importance above and below the channel layer.

After removal from the MBE reactor, samples were taken off their Mo blocks. They were then mounted on glass slides with wax and etched in HCl to remove residual In from their backsides. Next, samples were mounted on a lapping jig and lapped for smoothness on their obverse sides to facilitate device fabrication.

HIGFET structures and Van der Pauw type five terminal configuration structures suitable for gated Hall and conductivity measurements were fabricated by optical lithography and lift-off techniques in the same manner. MIS-type transverse diodes were fabricated on layers grown on n-GaAs substrates and are discussed later. HIGFET device geometries consisted primarily of 2µm, 3µm, 5µm, and 110µm gate lengths. The 110µm gate length device represents a special oversized dimensioned HIGFET test device and is commonly referred to as a FATFET. Device fabrication requires a three-level mask process. The masks for the 2µm and 3µm gate length devices were commercially obtained and have a configuration shown in Fig. 5.4. The masks for 5µm gate length device were also obtained commercially and have a configuration illustrated by Fig. 5.5. While the FATFET has a configuration similar to the 5µm gate length device, the masks for this device as well as for various five terminal Van der Pauw patterns were designed and made at UCSD. Mesa patterns were etched using 38 H_3PO_4: 1 H_2O_2: 1 H_2O. AuGe/Ni was thermally evaporated, defined, and annealed for ohmic contacts. Finally, aluminum was vacuum deposited and defined to form the gate electrodes and contact pads.

Electrical measurements were made on the completed HIGFETs by means of Tektronix/Sony Type 370 and 576 transistor curve tracers. Individual devices were

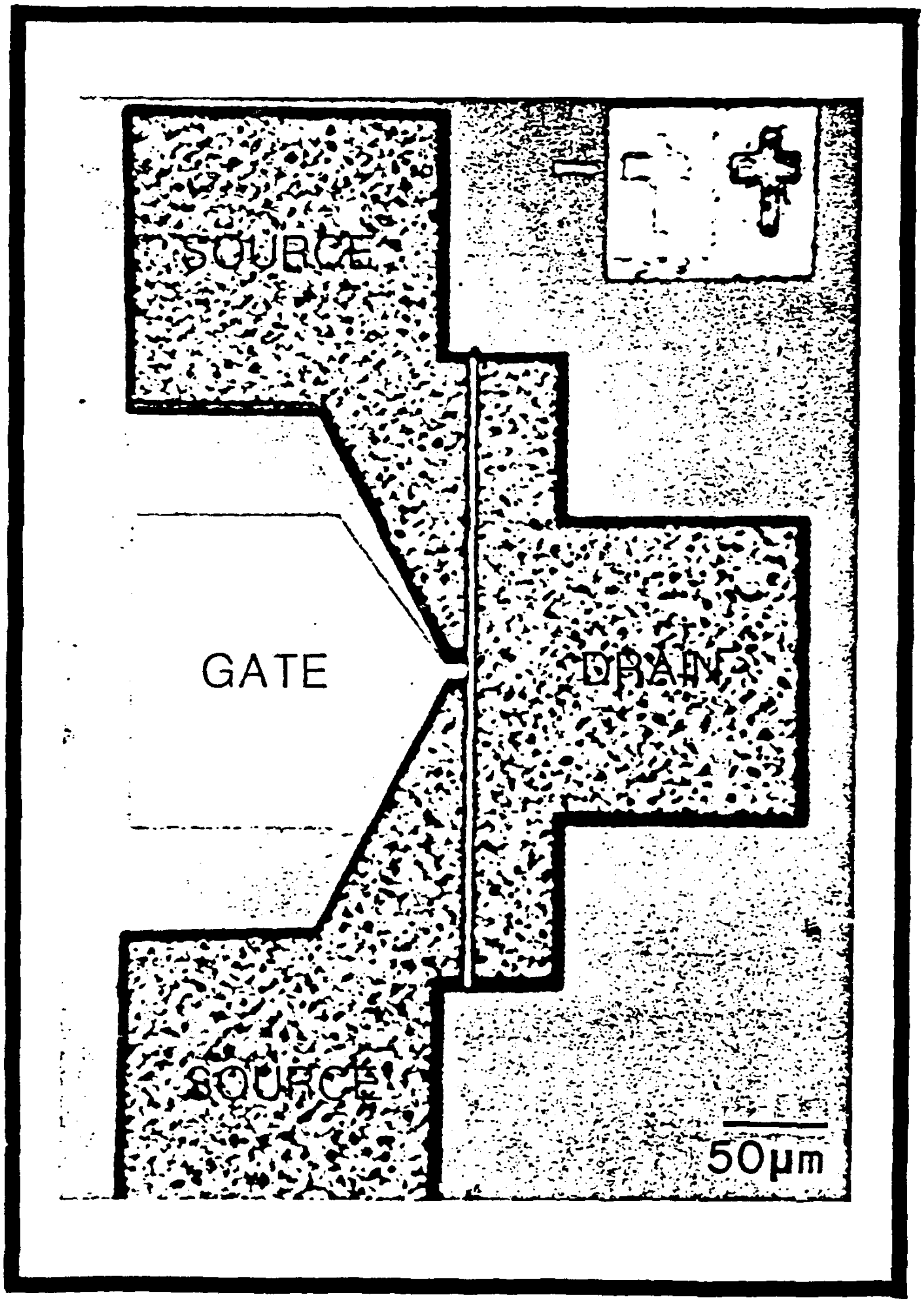
SOURCE
GATE
DRAIN
SOURCE
50μm

Figure 5.4: Photomicrograph of a completed 2μm gate length HIGFET after using a three-mask photolithographic and lift off process to form mesa, ohmic contacts, and gate electrode. This device uses a split source configuration.

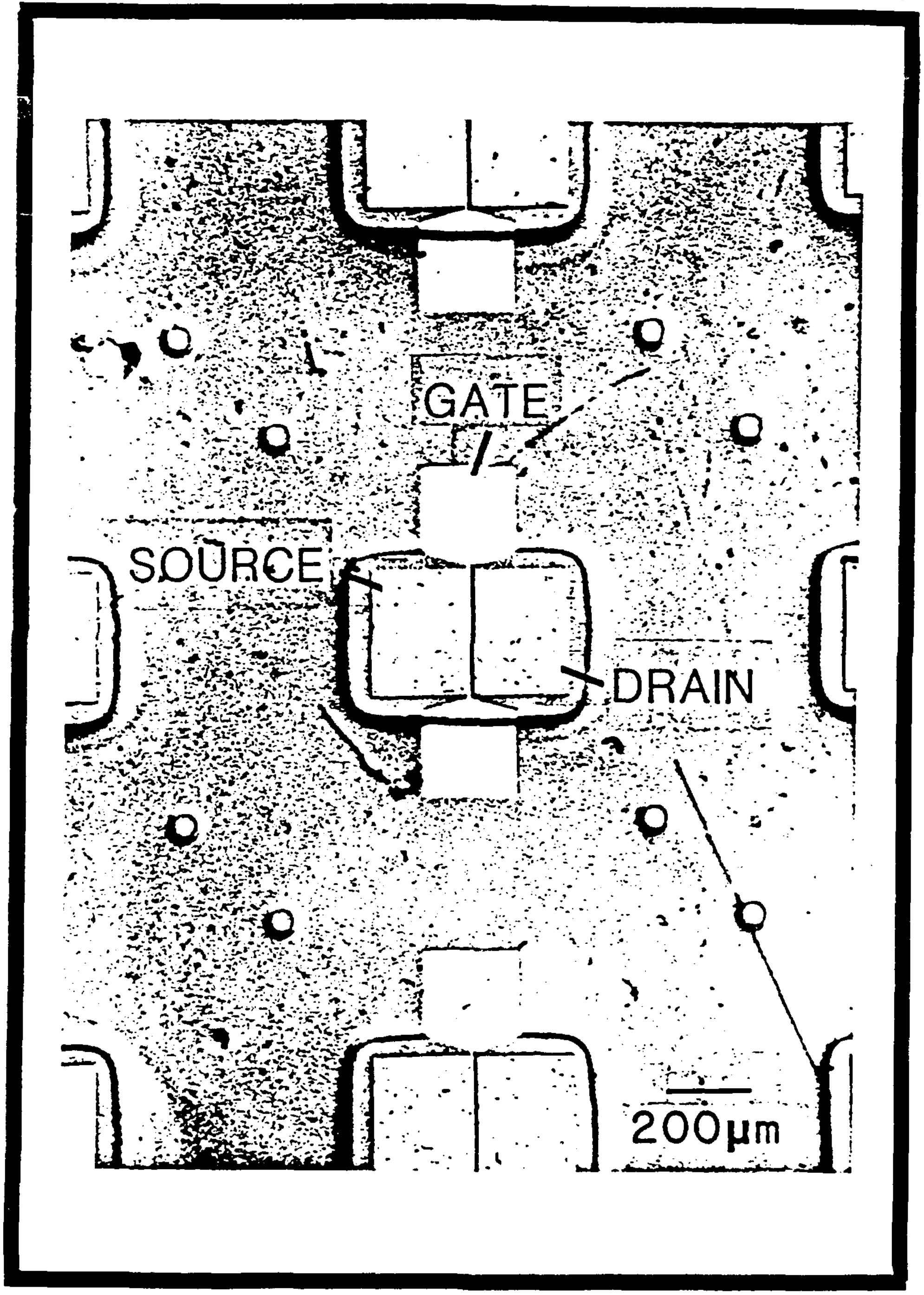
GATE
SOURCE
DRAIN
200μm

Figure 5.5: Photomicrograph of a completed 5μm gate length HIGFET after using a three-mask photolithographic and lift off process to form mesa, ohmic contacts, and gate electrode.

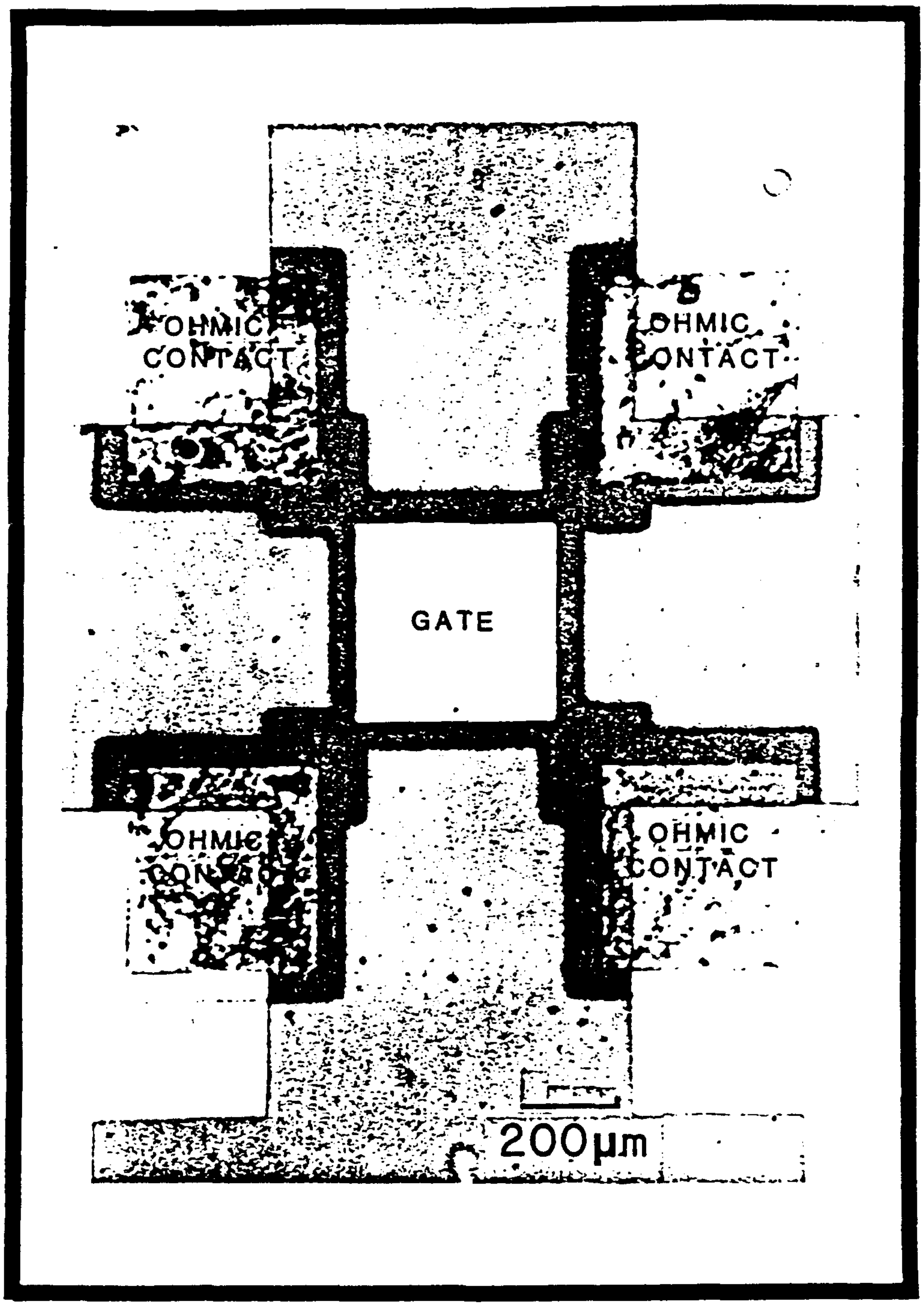
OHMIC CONTACT
OHMIC CONTACT
GATE
OHMIC CONTACT
OHMIC CONTACT
200µm

Figure 5.6: Photomicrograph of a completed five terminal Van der Pauw configuration test device after using a three-mask photolithographic and lift off process to form mesa, ohmic contacts, gate electrode, and contact pads. The device has four corner ohmic contacts and a central gate contact.

electrically contacted by probes. Hall and conductivity measurements were made using variable DC currents and a reversible pole permanent magnet as well as by a double AC Hall apparatus designed and built at UCSD.[6] Samples were mounted into specially prepared dual in-line packages (DIPs) which are fitted into the Hall apparatus at UCSD. Contacts to the four ohmic contact pads were made by using In solder. A mechanical contact to the central gate pad of the Van der Pauw pattern is made by a spring loaded Au-Ni wire attached to the DIP. This mechanical contact can be then enhanced by

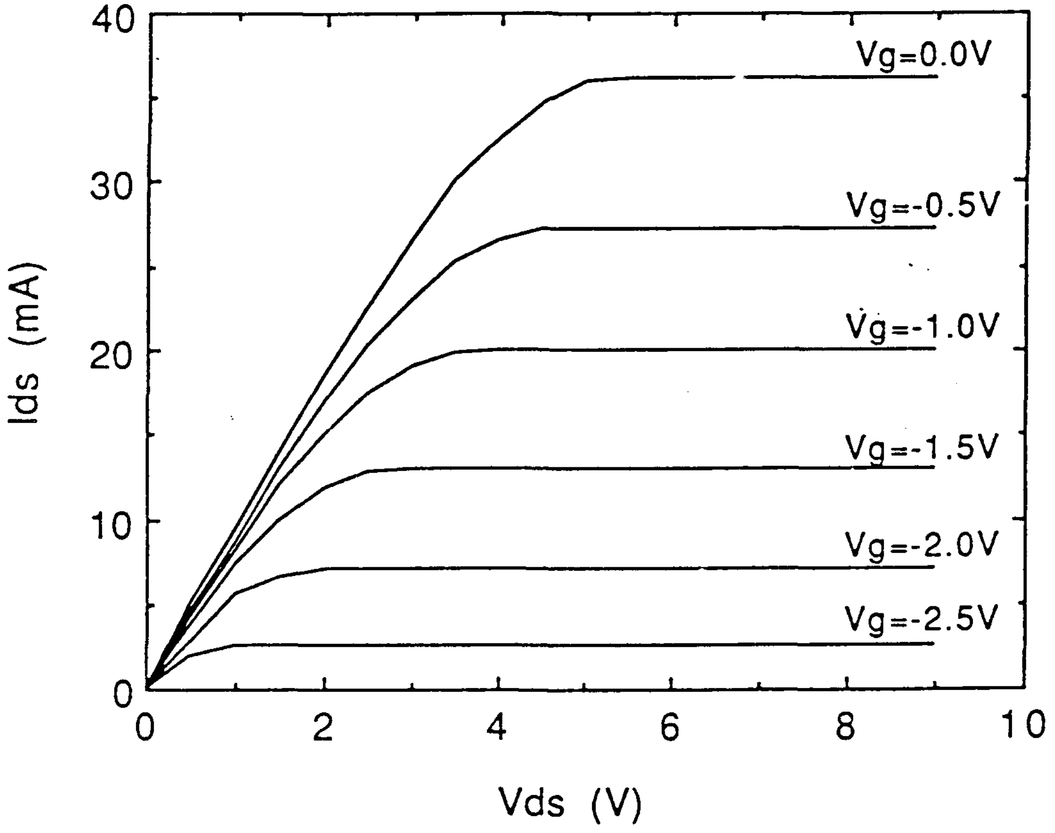

Figure 5.7: Drain characteristics of the depletion-mode HIGFET shown in Fig. 5.3, having L_g=5μm, W_g=280μm, and L_{sd}=16μm at 300K without illumination.

applying colloidal silver to the contact point. A typical five terminal Van der Pauw pattern is shown in Fig. 5.6. Hall and conductivity measurements on ungated devices yield typical values for the channel electron density and mobility of $n=3.8\times10^{18}$ cm^{-3} and $\mu_n=2000$ cm/V-sec, respectively. These values are strongly consistent with those indicating a degenerate electron distribution and dominant impurity scattering.

The drain characteristics of a typical depletion-mode HIGFET (whose cross-section was shown in Fig. 5.3) is shown in Fig. 5.7. The device demonstrates good saturation and pinch-off of the drain currents. The highest observed extrinsic saturated transconductance, g_m, observed for a gate length of 2μm at $V_g= 3$V and $V_{ds}= 2.5$V was 140 mS/mm. The reverse gate leakage current was less than 0.1μA for gate biases, $V_g\leq-5$V, and the pinch-off voltage, V_p is ~-4.5V.

Non-uniform Channels

An initial examination of the transistor I-V characteristics suggests that the source-drain conduction path is not limited to the heavily doped n$^+$-type $In_{0.30}Ga_{0.70}As$ channel layer but that the undoped $In_{0.15}Ga_{0.85}As$ buffer immediately below the channel layer also plays a significant role in the conduction process. If the conduction band discontinuity is ignored at the n$^+$-$In_{0.30}Ga_{0.70}As$ channel-undoped $In_{0.15}Ga_{0.85}As$ buffer interface, then the channel may be thought to be composed of the original 150Å n$^+$-doped channel and an electron distribution, n(x), stretching into the buffer an unspecified depth. Together, the entire channel may be considered to have a non-uniform doping profile.

In order to properly determine the parameters needed to model the device, knowledge of the doping density and electron concentration profile must be obtained. The modelling of non-uniformly doped FET channels has been described by others, with particular emphasis on ion-implanted FETs.[7,8] The electron concentration profile has been derived by two methods: a) experimental C-V measurements have been made and an electron concentration profile derived; and b) the theoretical electron distribution for a high-low junction has been predicted.

Capacitance vs. Gate Voltage Measurements

In order to determine the electron density profile of the structures employed for HIGFETs, a differential capacitance-voltage (C-V) technique was applied to specially fabricated transverse MIS-type diodes. Substrates of n-type GaAs were introduced side-by-side on the same Mo blocks with semi-insulating GaAs substrates, intended for HIGFET structures, in the MBE reactor. As a result, layers grown on the n-type substrates are exactly the same as produced on the semi-insulating substrates. Once removed from the MBE reactor, these n-type substrates underwent photolithographic processing by having circular Al contacts thermally evaporated onto their surfaces. A backside ohmic contact was made using In and the devices were mounted on Cu blocks to facilitate easy electrical probing. The C-V measurements were made at UCSD by means of either a Boonton Model 72B capacitance meter or a HP 4277A LCZ Meter. Data acquisition is simplified by the interface of either measurement package to a desktop HP 87XM computer.

The differential capacitance technique involves the sweeping of the space-charge depletion layer in the MIS capacitor through the region with the unknown carrier profile by applying a variable bias voltage. The validity of the C-V method of measurement of the impurity profile or electron concentration is based upon the depletion approximation. The depletion approximation assumes that there is a sharp interface transition at the edge of the space-charge region and that the space-charge region contains only the charge due to ionized impurities. In other words, it assumes the Debye length, L_D, which is defined as

$$L_D = \left(\frac{kT\,\varepsilon_s}{q^2 N} \right)^{1/2} , \tag{5.1}$$

has a zero value. The doping profile, N(x), can be obtained from the capacitance measured as a function of bias voltage. However, Kennedy, Murley, and Kleinfelder[9] have shown that the profile obtained is not that of the dopant profile but rather that of the free carriers. While in many cases the dopant profile and electron concentration profile may coincide, it is not always true. The electron concentration, n(x), may be determined from C-V measurements as

$$n(x) = \frac{2}{q\varepsilon_s A^2} \left[\frac{d(1/C_m^2)}{dV} \right]^{-1} , \tag{5.2}$$

where q is the electronic charge, ε_s is the dielectric constant of the semiconductor, A is the diode area, and C_m is the total measured capacitance. The depth, x, is determined from

$$x = \frac{\varepsilon_s A}{C_s} = \varepsilon_s A \left(\frac{1}{C_m} - \frac{1}{C_i} \right) , \tag{5.3}$$

where C_s is the capacitance of the depletion layer in the semiconductor. C_i is the capacitance per unit area of the insulator and is defined as

$$C_i = \frac{\varepsilon_i}{d_i}, \tag{5.4}$$

where ε_i is the dielectric constant of the insulator and d_i is the thickness of the insulator.

The application of differential C-V measurements to determine non-uniform doping profile is related to work performed earlier by others on ion-implanted devices[10,11] and current investigations underway on delta-doped structures.[12] Both types of structures deal typically with narrow doping peaks and large doping steps. The C-V technique has been used to gain information about their dopant profiles and free carrier profiles. The properties of some ion-implanted FETs are expected to be very similar to the structures described here since they involve the introduction of a heavily doped channel layer into a relatively low, undoped region. MBE growth provides some advantages compared to ion implantation by allowing the introduction of a heavily doped region *in situ* . It does not induce any lattice damage which requires annealing to repair the lattice damage such as ion implantation does. Furthermore, by avoiding such a thermal anneal, the MBE grown structure does not undergo possible spatial redistribution of impurities as is often the case in ion implanted structures.

Figure 5.8 shows a typical capacitance vs. voltage plot and Fig. 5.9 shows a typical electron concentration versus depth profile as obtained by using equations 5.2 and 5.3. The slope of the 1/C versus V is calculated by taking the slope between every point and assigning it to the average value of the voltage between those two points. Because of the lack of available knowledge regarding the $In_xAl_{1-x}As$ properties, the zero bias voltage capacitance is taken to be the capacitance of the quasi-insulator. This is not unreasonable because the structure is expected to be, to first order, at flat band for zero bias voltage. The presence of such a heavily doped $In_{0.30}Ga_{0.70}As$ layer adjacent to the $In_{0.15}Ga_{0.85}As$ cap would suggest either no depletion or a negligibly small depletion. Similarly no significant accumulation would exist if the conduction band discontinuity were considered to be of importance since the cap is undoped and would contribute only a negligible number of carriers. Thus the zero voltage bias capacitance is considered to only reflect the quasi-insulator layer. A divergence between the observed capacitance and the calculated geometric capacitance of the insulator layer, determined from equation 5.4 using d_i as calculated from growth parameters and e_i, calculated from an interpolation between the dielectric constants of InAs and AlAs, can be expected because

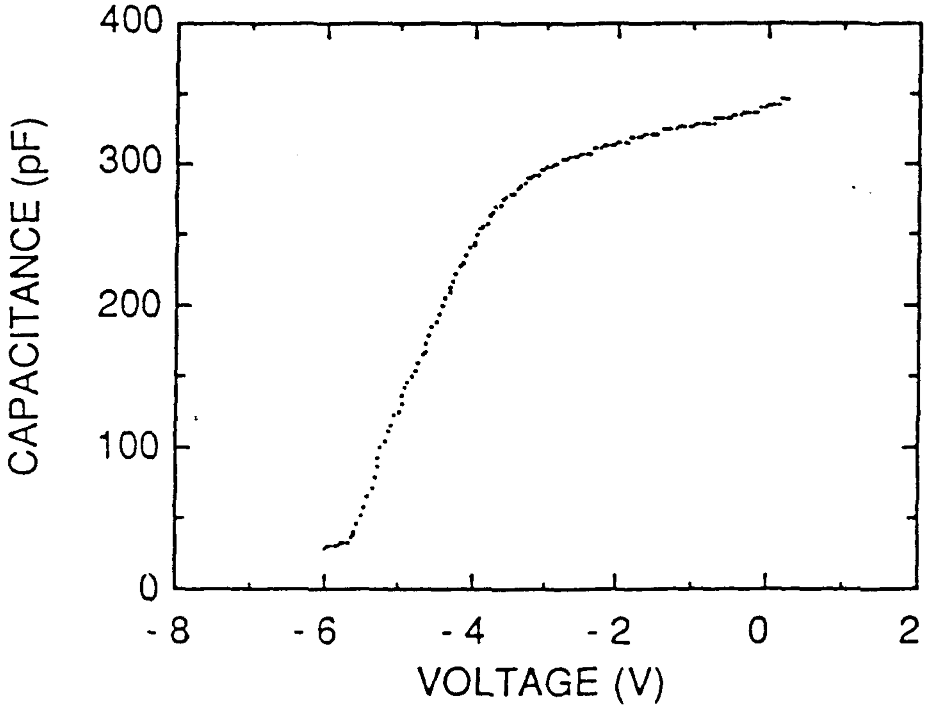

Figure 5.8: Typical C-V curve obtained for a HIG capacitor grown simultaneously with FET structures. Taken at 300K without illumination.

the precise dielectric permittivity of the layer is unknown. The profile shows a rapid decrease from the high side of the heterojunction with a long tail into the low side. The low side appears to have a residual doping of about n=7x10^{14} cm^{-3}. This is in agreement with Hall measurements which were made on layers grown without a channel or cap. Consisting of only the buffer layers grown on semi-insulating substrates, the Hall measurements indicate a carrier concentration

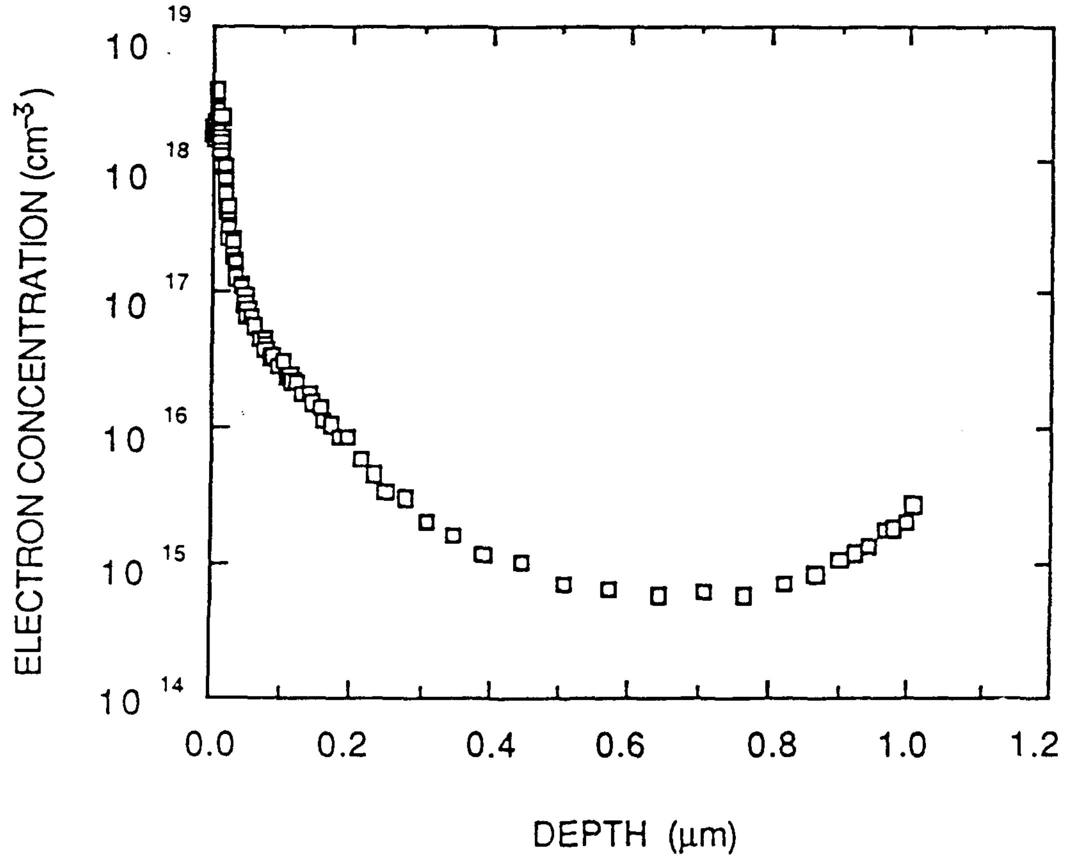

Figure 5.9: Carrier profile as determined from the C-V data in Fig. 5.8.

$n<5\times10^{15}$ cm^{-3}. The increase in the carrier concentration profile deep within the structure is that of the n^+-type substrate.

A preliminary study of the possible effect of interface states on the C-V profile is shown in Fig. 5.10 and 5.11. If the interface state density is large, a wide dispersion in the C-V data would be expected for changes in the a.c. probing frequency. However, Fig. 5.10 shows only small dispersion. Fig 5.11 shows that there is

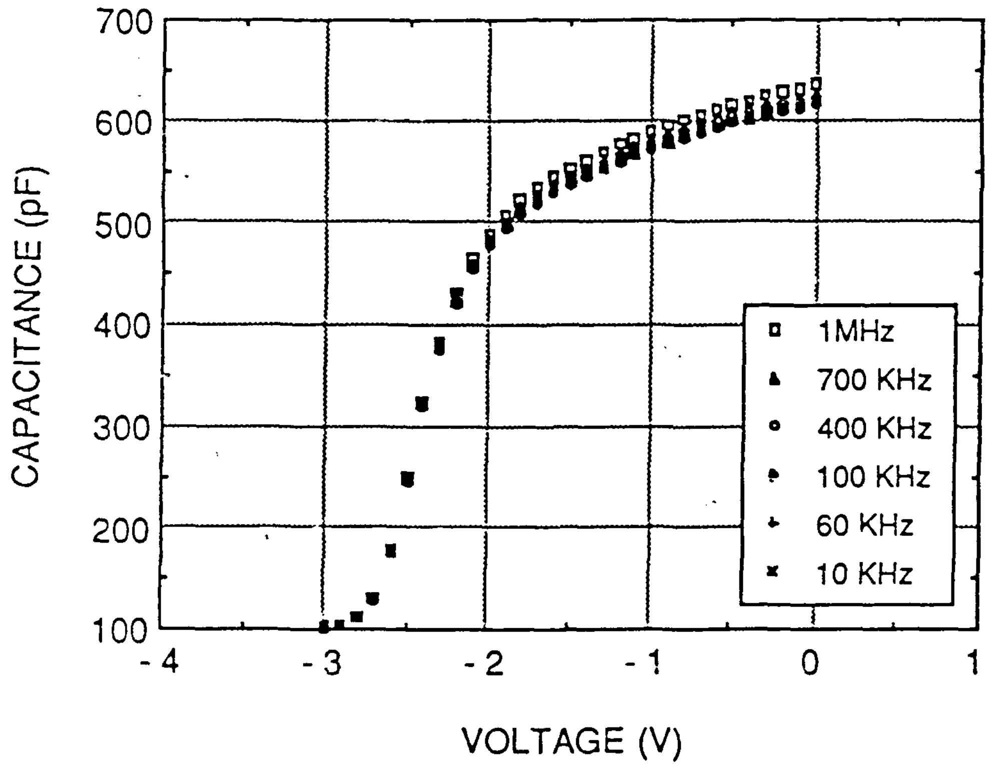

Figure 5.10: Typical dispersion of the C-V data for an a.c. probing frequency of 1MHz, 700KHz, 400KHz, 100KHz, 60KHz, and 10KHz, taken at 300K without illumination.

no dispersion with fast D.C. sampling times. Thus the C-V measurement does not appear to be affected to a significant degree by the presence of interface states. Interface states might, perhaps, play a more dominant role if the Fermi-level at the interface were nearer to midgap, or if deep states were distributed over most of the fundamental bandgap. The channel is heavily doped and probably degenerate, thus the effect of interface states are considerably reduced.

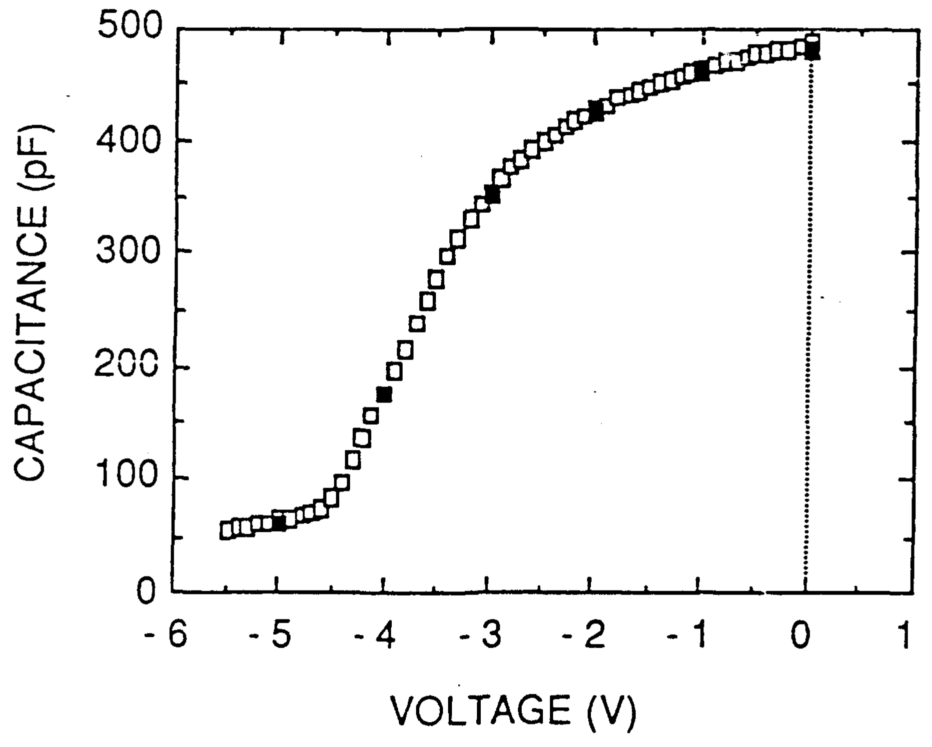

Figure 5.11: Typical dispersion of the C-V data for a high speed d.c. sweep (closed square) and standard d.c. sweep (open square) using an a.c. probing frequency of 1MHz at 300K without illumination.

The C-V technique is just one of the available methods for profiling a transistor channel. The profile derived will be utilized to model the transistor I-V curves. However, C-V techniques do have drawbacks. Johnson and Pancusis[13] found that because the electron density may change over a width of several Debye lengths when the bias voltage is changed, the resulting spatial resolution severely limits the accuracy of the C-V measurement and that the measured C-V profile will differ from the true majority carrier concentration. Thus the assumption of a zero Debye length when calculating the doping profile from C-V data of regions with large gradients will lead to errors. Other work by Wu *et al.*[14] on ion-implanted profiles shows severe limitations in the C-V technique and the amount of useful information it provides. In the next section, a standard high-low junction profile is examined as an alternative model for the carrier concentration profile.

High-low Junction Profiling

The high-low (n^+-n^-) step junction such as that present within the structure means that consideration must be given to the carrier profile at equilibrium, which may not be the same as that of the impurity profile. We consider the case of a very abrupt spatial variation in doping with no observable dopant diffusion. In the high-low junction, the heavily doped "high" side is slightly depleted at its interface while on the "low" side accumulation, with respect to the background electron density, takes place. As in a p-n junction, a dipole layer is formed such that the depletion charge consists purely of fixed ionic charge on the high side balanced by mobile majority carriers (accumulation) on the low side. In grossly asymmetric high-low junctions the high side exhibits a potential drop of only kT/q, this being independent of the doping nature on the low side; almost all of the potential drop occurs on the low side of the junction.

Following the work on high-low junctions presented by Warner and Grung[15], the potential, and hence the charge distribution, with respect to position from the junction may be determined. This is a simple one-dimensional case which can be used to solve for the potential as a function of depth relative to the interface. A schematic of the energy band structure with respect to the interface is shown in Fig. 5.12. Far from the interface, the electron density is independent of position and coincides with the impurity density. These bulk-region doping values were determined by means of Hall

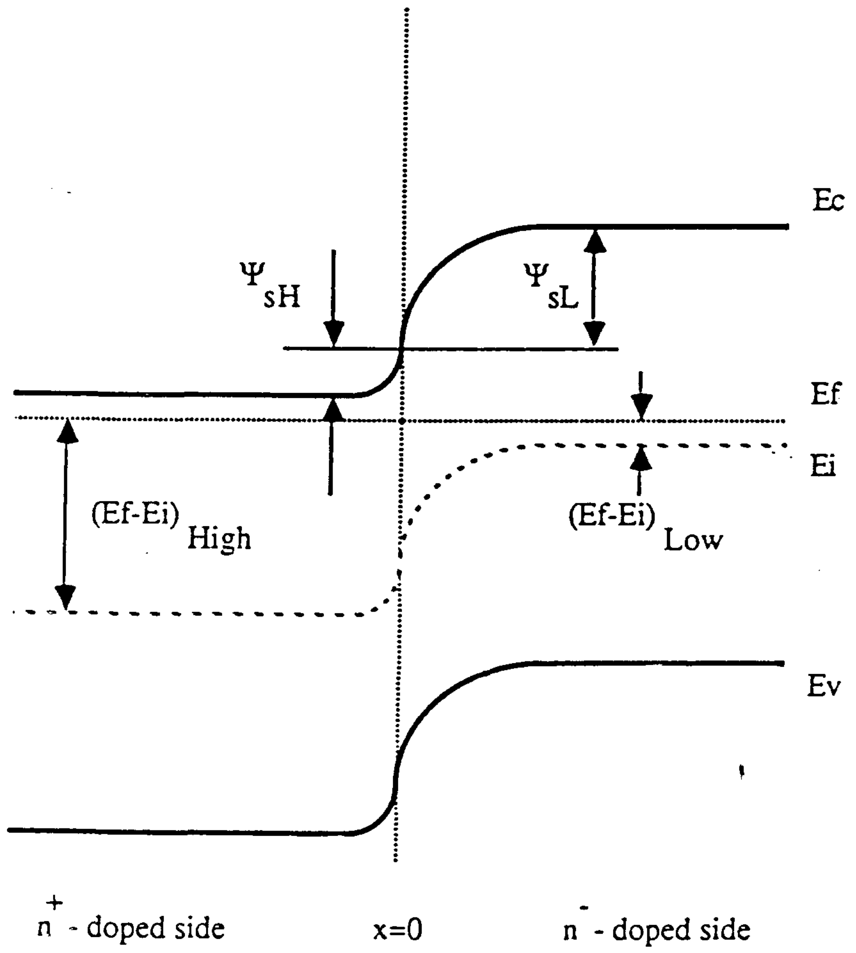

Figure 5.12: Schematic diagram of the energy band structure for an abrupt high-low junction.

measurements on similar thick layers grown separately and by means of the C-V measurements described earlier. The C-V profile is fairly reliable for providing the electron concentration information as long as it is measured several Debye lengths from any interface.

Assuming that the Boltzmann approximations are applicable, then the total electrostatic potential due to the junction may be given as

$$\left|\Psi_{sH}\right| + \Psi_{sL} = (E_f - E_i)_H - (E_f - E_i)_L = kT \ln \frac{N_{DH}}{N_{DL}} \tag{5.5}$$

where E_f is the Fermi-level, E_i is the intrinsic Fermi-level, N_{DH} and N_{DL} are the bulk doping densities in the high and low regions, respectively, and Ψ_{sH} and Ψ_{sL} are the potentials at the junction on the high and low sides, respectively. The potential as a function of distance, $\Psi(x)$, may be obtained from the one-dimensional Poisson's equation

$$\frac{d^2}{dx^2}\Psi(x) = -\frac{\rho(x)}{\varepsilon_s}, \tag{5.6}$$

where ε_s is the permittivity of the semiconductor and $\rho(x)$ is the space-charge density which may be approximated for the abrupt junction as

$$\rho(x) = q\,(N_D - n(x)). \tag{5.7}$$

The term $n(x)$ may be written as

$$n(x) = n_i \exp\left(\frac{E_f - E_i}{kT} + \frac{q\,\Psi(x)}{kT}\right) = N_D \exp\left(\frac{q\,\Psi(x)}{kT}\right), \tag{5.8}$$

where n_i is the intrinsic carrier density. Plugging back into Eq. 5.6, the resultant Poisson's equation is

$$\frac{d^2\Psi(x)}{dx^2} = \frac{q\,N_D}{\varepsilon_s}\left[\exp\left(\frac{q\,\Psi(x)}{kT}\right) - 1\right]. \tag{5.9}$$

Integrating this equation will give the relation between the electric field, E, and the potential:

$$E(x) = -\frac{d\,\Psi}{dx} = -\left(\frac{2kT}{\varepsilon_s}\right)^{1/2}\left\{N_D\left[\exp\left(\frac{q\,\Psi(x)}{kT}\right) - \frac{q\,\Psi(x)}{kT} - 1\right]\right\}^{1/2}. \tag{5.10}$$

Since the electric displacement vector must be continuous across the junction then the low-side electric displacement term must equal the high-side electric displacement term at the interface. Thus,

$$\varepsilon_{sH}\,N_{DH}\left[\exp\left(\frac{q\,\Psi_{sH}}{kT}\right) - \frac{q\,\Psi_{sH}}{kT} - 1\right] = \varepsilon_{sL}\,N_{DL}\left[\exp\left(\frac{q\,\Psi_{sL}}{kT}\right) - \frac{q\,\Psi_{sL}}{kT} - 1\right], \tag{5.11}$$

from which Ψ_{sH} and Ψ_{sL} can be determined. Taking Eq. 5.10 and integrating once more will give the relation between potential and distance from the junction, x, as

$$x_{(i+1)} = -\left[-x_i + \int_{\Psi_{(i)}}^{\Psi_{(i+1)}}\left\{\frac{2kT}{\varepsilon_s}N_D\left[\exp\left(\frac{q\,\Psi}{kT}\right) - \frac{q\,\Psi}{kT} - 1\right]\right\}^{-1/2} d\Psi\right]. \tag{5.12}$$

This equation may be applied to each side of the junction separately using the boundary conditions $x_0 = 0$ and $\Psi_0 = \Psi_{sH}$ or Ψ_{sL} depending on which side of the junction is being examined.

The numerically calculated high-low step junction electron concentration profile is plotted in Figure 5.13. The high-low junction calculation uses a doping concentration of 4×10^{18} cm^{-3} for the high side and a low side doping of 7×10^{14} cm^{-3}. In plotting this figure, the high-side layer is only 150Å thick and simulates the n-

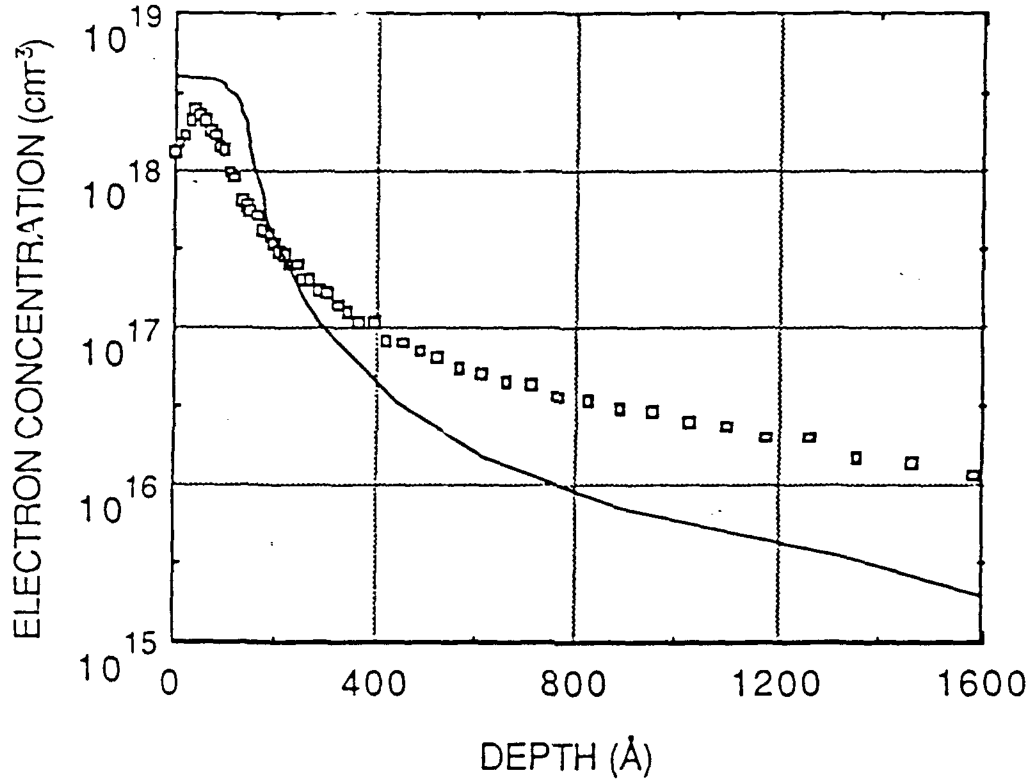

Figure 5.13: Electron concentration profile (solid line) as determined from a high-low step-junction calculation using 4×10^{18}cm^{-3} for the high region and 7×10^{14}cm^{-3} for the low region. For comparison, the profile obtained from the C-V data (open squares) is plotted as well.

$In_{0.30}Ga_{0.70}As$ layer as grown for the FETs. Also shown for comparison in Fig. 5.13 is the profile obtained from C-V measurements (plotted previously in Fig. 5.9). It is evident from the figure that the high-low profile shows the electron concentration to be confined closer to the junction than that of the C-V profile.

Modelling

A one-dimensional analytical model by Hill[16] has been applied to MISFET and HIGFET devices and will be used here as well. This model is derived from the work of Lile[17] and Pucel *et al.*[18] Pucel and coworkers developed a two piece approximation for one-dimensional electron transport in FETs, dividing the transistor characteristics into a linear (gradual channel) and saturation region. Lile's work involved an adaptation which includes the determination of the surface potential for insulated gate devices and consideration for the effect of insulator/channel surface states on the transistor properties. The generalizations of these relations in the Hill model allows for a simple, attractive description of the I-V dependence on gate voltage for MIS-type devices which includes the effects of the gate insulator properties on its I-V characteristics. Hill defines MIS as an "insulator-assisted" gate where the gate metallization is isolated from the semiconductor surface by a dielectric layer. The model may be reduced to the MESFET case when the insulator is reduced to zero thickness. This model offers the device designer a broad range of input parameters such as geometry, carrier concentrations, channel and insulator thicknesses and material properties, as well as anticipated surface state density and parasitic resistances.

The FATFET is a simple HIGFET test transistor with oversized dimensions. It is processed in exactly the same manner as the HIGFETs discussed in section 5.3 and is intended as a test device for examining material and processing parameters. The

FATFET has a gate length of 110 μm and a gate width of 425 μm. The source-drain separation is 175 μm, with the gate centered in the middle of this spacing. All I-V characteristics that were modelled were compared to FATFET results. The large size of the FATFET, compared to the 2μm FET, allows for a smaller error when determining dimensions and variations in dimensions. A typical I-V characteristic is shown in Fig. 5.14. FATFET I-V characteristics demonstrate good saturation and pinch-off and are

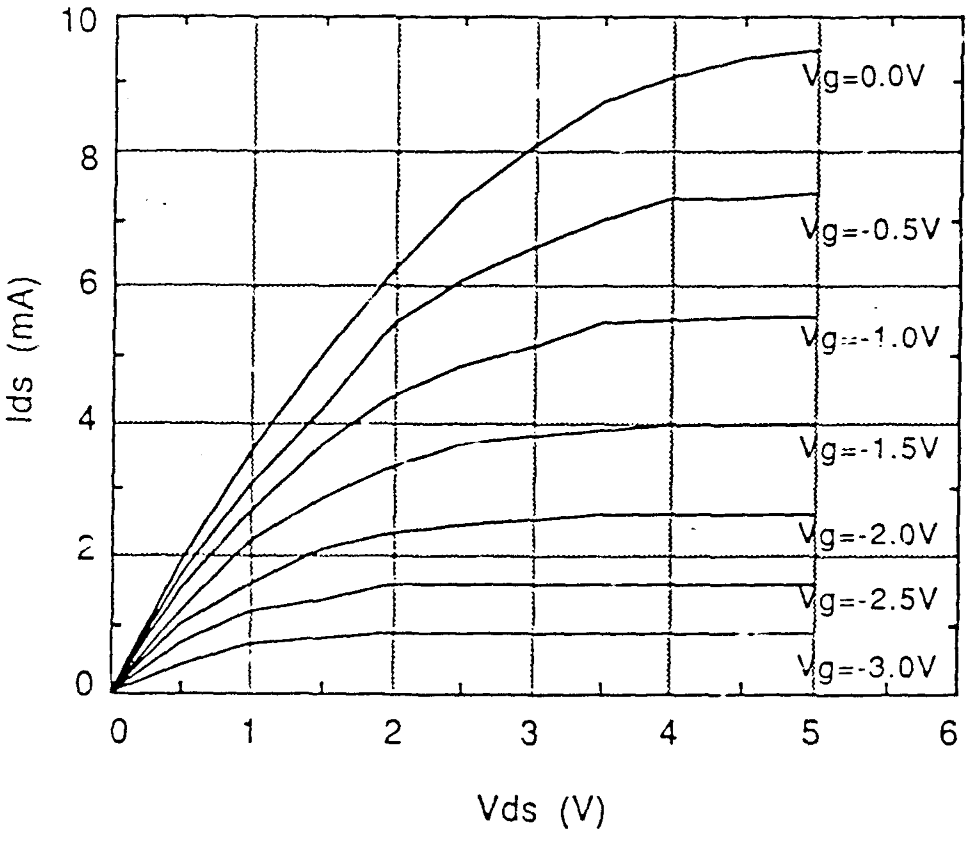

Figure 5.14: FATFET drain characteristics of the depletion-mode HIGFET shown in Fig. 5.3, having gate steps of -0.5V at 300K without illumination. The FATFET has L_g=110μm, W_g=425μm, and L_{sd}=175μm.

very reproducible, with little or no variation when illuminated.

The Hill model was applied by Hanson[1] to InAlAs/InP HIGFETs. The Hill model requires a number of input parameters. Basic geometric dimensions, from which theoretical source-drain resistances may be automatically determined, were measured optically. The dielectric constants were determined by a linear interpolation from values given in Sze[19] and Adachi. Thicknesses were calculated from growth rates which were determined by RHEED intensity oscillation measurements prior to the MBE growths. Electric field at peak carrier velocity and the saturation carrier velocity were taken from Masselink's data[20] for GaAs. The built-in surface potential is assumed to be zero since the device is thought to be at flat band at zero gate voltage. The initial surface state density has been set to zero. They are not likely to be greater than 1×10^{11} cm^{-2} and do not play a significant role until greater than 1×10^{12} cm^{-2} as shown by Hile. The C-V results discussed earlier suggest that this is the case. The remaining parameters include doping concentration and mobility. The doping concentration in the channel will be discussed in more detail shortly. From the last section it is clear that the doping is not uniform. The Hill model assumes uniform doping of the channel so some steps must be taken to deal with such a nonuniformity. The mobility represents an almost independent variable for adjusting the modelling results. However, it must remain in reasonable proportions. Figure 5.15 plots the expected mobility for GaAs based upon Hilsum's equation[21],

$$\mu = \frac{\mu_0}{\left[\, 1 + (n / n_0)^{g} \,\right]}, \qquad (5.13)$$

with the numerical values $\mu_0 = 8500$ cm^2/V-sec, $n_0 = 10^{17}$ cm^{-3}, and $g = 0.5$, and Walukewicz's results[22] with a compensation ratio of 0.5. This plot represents values which might be expected for the Hall mobility with which the model should reasonably concur.

Although many methods were attempted only three results will be reported here. All three methods use the same Hill model program but vary in their approach

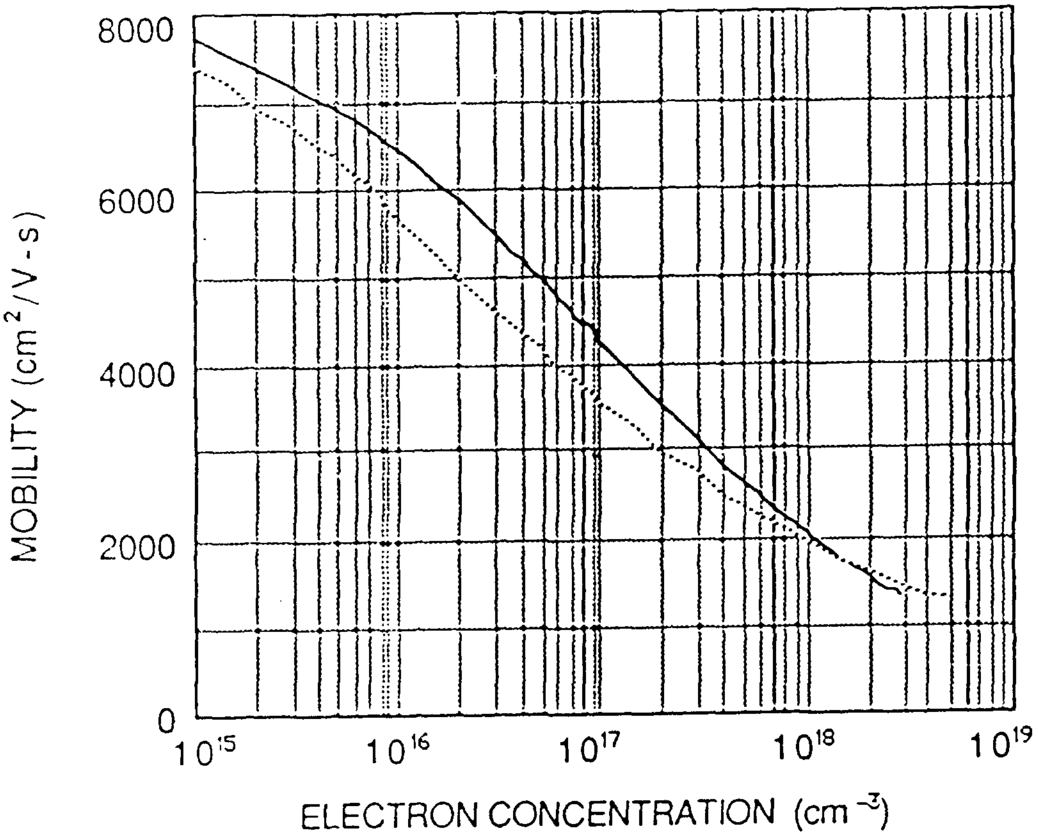

Figure 5.15: Variation in the mobility as a function of impurity doping concentration for GaAs at 300K taken from the data of Walukiewicz *et. al.* (Ref. 22) for a compensation ratio of 0.5 (dotted line) and from the Hilsum model (Ref. 21) using $\mu=8500/(1+N_d/1\times10^{17})^{1/2}$ (solid line).

intended to account for the nonuniform doping distribution in the channel. The first method utilized a single averaged doping concentration over a specifically chosen depth. The second method utilizes the carrier profile obtained from the C-V technique, first using a trapezoidal method to approximate the profile and next using an analytic function to approximate the profile. Either method of approximating the profile allows one to calculate the average channel carrier concentration with respect to varying gate voltages. Finally, the last method uses the carrier profile obtained from the theoretical high-low junction calculations. Again an analytical expression which provides a reasonable approximation of the curve is determined and subsequently used to calculate the average carrier concentration as a function of gate voltage.

Method A

The Hill model contains the initial assumptions of a uniformly doped channel, the applicability of Poisson's equation, and that of Gauss' law in determining an effective surface potential. With these assumptions it is possible to calculate the expected depletion depth of the channel. The depletion depth with respect to channel position must be calculated in order to determine the drain current. Similarly, a uniform doping is used in this model for calculating the pinch-off voltage.

A single average doping density has been used by Shur and Eastman[23] to profile ion-implanted MESFETs. This simple approximation of an ion-implanted doping profile yields fairly reasonable results despite the very nonuniform appearance in the measured profile. In order to fit the data of Fig. 5.14, the mobility and channel depth must be chosen to provide realistic values for the I-V characteristics. The approximation of the doping profile using the method described by Shur and Eastman is shown in Figure 5.16 and is plotted with the results from the C-V measurement profile for comparison. The approximation is then used to help fit the transistor data using Hill's model and the result of this fit is shown in Figure 5.17. It should be noted that the number of gate voltage steps is limited by the channel depth and carrier concentration chosen. The carrier concentration, in turn, affects the pinch-off voltage. Other attempts to generate similar I-V characteristics show that the number of gate voltage steps is

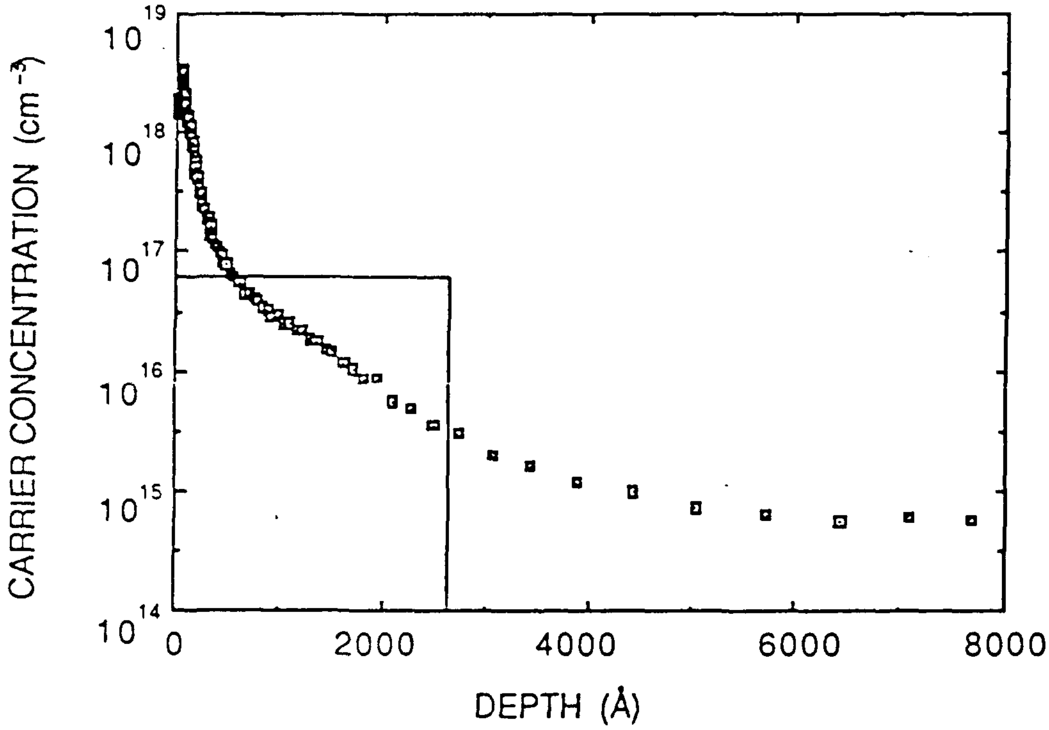

Figure 5.16: Approximation of the doping profile using a single average doping density over a fixed channel depth (solid line). Plotted for comparison is the doping profile determined experimentally from C-V measurements (shown as the open squares).

related to the carrier concentration chosen. More gate voltage steps occur before pinch-off with lower carrier concentrations. The lower carrier concentration dictates a thicker channel depth in order to fit the experimentally observed current and this increase in thickness, in turn, allows more gate voltage steps to take place before pinch-off. The fit shown utilizes a doping concentration of 5.92×10^{16} cm^{-3}, a channel depth of 2650Å, and a mobility of 8400 cm^2/V-sec. As stated previously, the electric field at peak carrier velocity and saturation carrier velocity are taken from Masselink's data and are

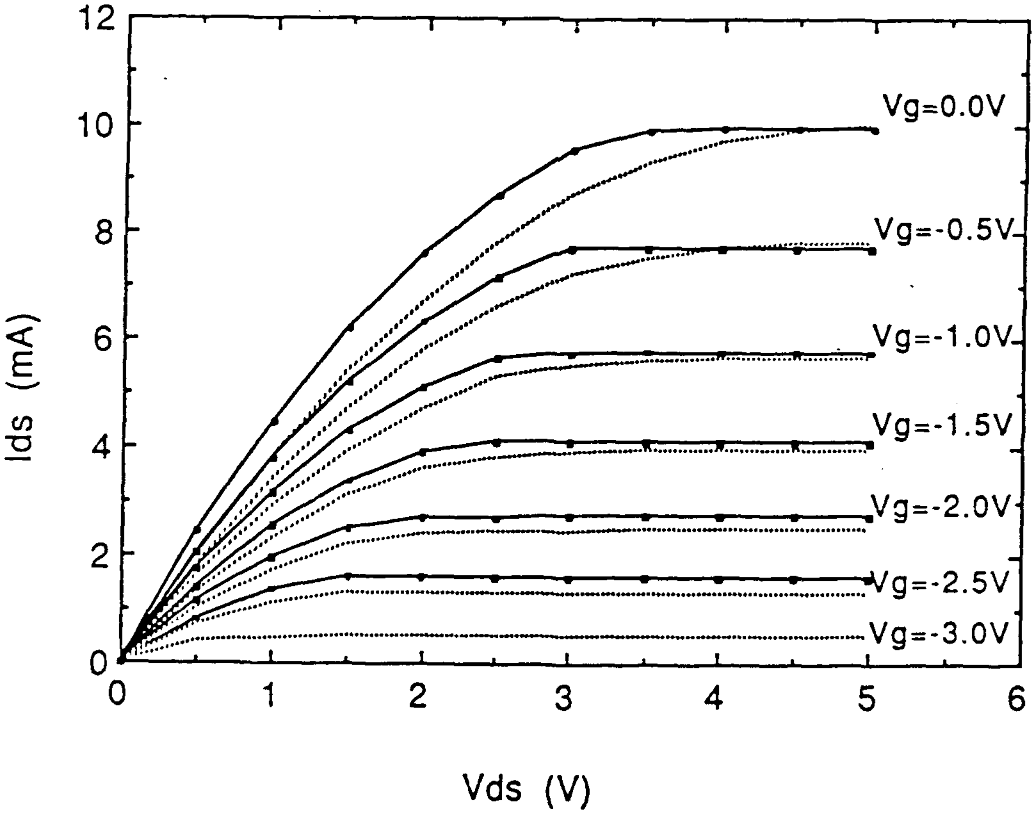

Figure 5.17: Fit of model A using the Hill model program to the measured FATFET I-V characteristics. The solid line is the fitted transistor data and the dotted line is the measured I-V data.

dependent on the carrier concentration chosen. The surface state density is chosen to be zero.

Model B and Model C

It is possible to determine the behavior of the depletion region for a nonuniformly doped channel by breaking the carrier profile with respect to depth into small trapezoids. From each trapezoid an average doping concentration may be obtained from which the model's depletion movement may be plotted. From Hill, the depletion depth, h, behaves as,

$$h = \left[\frac{-V_i^{1/2} + (V_i - \beta(K_0 + V_{gs}))^{1/2}}{\beta V_p^{1/2}} \right] a , \tag{5.14}$$

with,

$$V_i = \frac{q\,\varepsilon_s N_d t^2}{2\,\varepsilon_i^2} , \tag{5.15}$$

$$V_p = \frac{q N_d a^2}{2\,\varepsilon_s} , \tag{5.16}$$

$$K_0 = \beta \psi_{s0} - 2 \left(V_i \left| \psi_{s0} \right| \right)^{1/2} , \tag{5.17}$$

and,

$$\beta = 1 + \frac{q\, t\, N_{ss}}{\varepsilon_i}, \tag{5.18}$$

where N_d is the doping concentration, N_{ss} is the surface state density, ψ_{s0} is the surface potential at zero gate voltage, t is the insulator thickness, and a is the active layer thickness, which will drop out since it is included in the pinch-off voltage term. Thus the depletion depth behavior may be determined for every trapezoid of doping N_d and width x.

The experimentally measured FATFET transistor I-V characteristic curves such as shown in Fig. 5.14 are plotted as a function of gate voltage which is stepped by 0.5 volts. Thus the depletion depth may be calculated for 0.5 volt steps. For each gate step the channel is reduced in thickness. The average doping concentration may be calculated by using the method of first moments on the remaining channel. The average doping, <n>, may be written as

$$\langle n \rangle = \frac{\sum_j n_j x_j}{\sum_j x_j}, \tag{5.19}$$

or

$$\langle n \rangle = \frac{\int n(x)\, dx}{\int dx}. \tag{5.20}$$

order to apply the Hill model, the depleted region may be thought of as being in ries with the quasi-insulator, in essence increasing the insulator thickness. Since the ulator material is considered only as a dielectric layer, the difference in dielectric constants may be taken into account by correcting for the insulator thickness. Thus, the insulator thickness, t, at any given gate voltage becomes

$$t = h\frac{\varepsilon_i}{\varepsilon_s} + t_0, \tag{5.21}$$

where t_0 is the $In_xAl_{1-x}As$ cap thickness and h is the depletion depth into the semiconductor. In the case where the depletion depth exceeds the $In_{0.30}Ga_{0.70}As$ channel layer, t becomes

$$t = \varepsilon_i\left(\frac{h_1}{\varepsilon_{s1}} + \frac{h_2}{\varepsilon_{s2}}\right) + t_0, \tag{5.22}$$

where h_1 is the thickness of the $In_{0.30}Ga_{0.70}As$ layer and h_2 is the thickness of the depletion region extending into the next region. In each case, the initial surface potential is considered to be zero, and a fit is obtained for each I-V curve (gate voltage step) separately, using the parameters calculated in the manner shown above. The other parameters are adjusted according to the <n> chosen.

Initially, the trapezoidal method was employed to determine <n>. However if an analytical expression may be found to approximate the profile, then a simple integration may be used instead. Figure 5.18 shows a plot of the analytical expression,

$$n = N_0\left(\frac{x_0}{x}\right)^k, \tag{5.23}$$

with $N_0=3\times10^{18}$ cm^{-3}, $x_0=60$Å, and $k=1.8$, which is chosen to replace the C-V profile. The general form of this expression is taken from the work of Shur and Eastman[23].

Excellent agreement can be found between the trapezoidal method and the integrated analytic function.

The final fit is shown in Fig. 5.19. The first 60Å of the profile is presented as a constant doping region of 4×10^{18} cm^{-3} and the remaining portion of the profile is represented by the function above. The fit is made by breaking the electron density profile into two regions. The head represents the portion of the channel closest to the

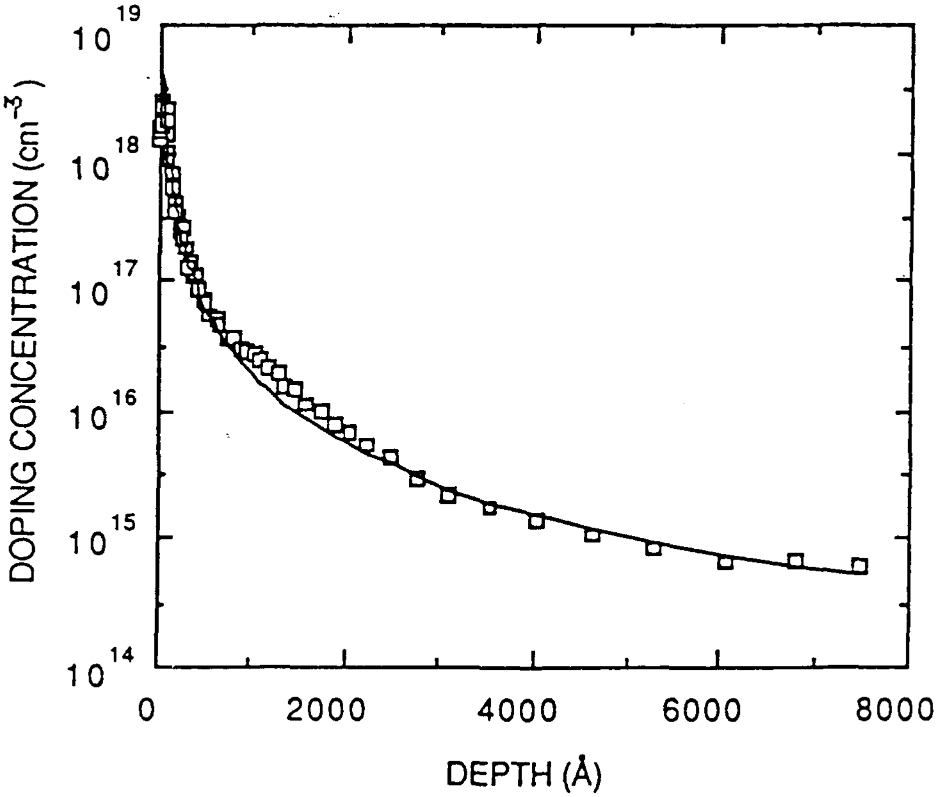

Figure 5.18: Comparison of the analytic function $n=3\times10^{18}(60/x)^{1.8}$ shown as a solid line and the profile obtained from the C-V data shown with open squares.

cap and the tail closest to the substrate. The overall channel is considered to be 1μm thick but the tail portion contributes only a small fraction of the current despite the large thickness associated with it. Thus the tail represents a baseline current value. The remaining thickness, set to about 500Å, is considerably smaller than the entire channel but most of the conduction and depletion due to applied gate voltage occur here. The resulting model shows an excellent fit for small gate voltages, with the fit worsening as the depletion depth nears the 500Å baseline.

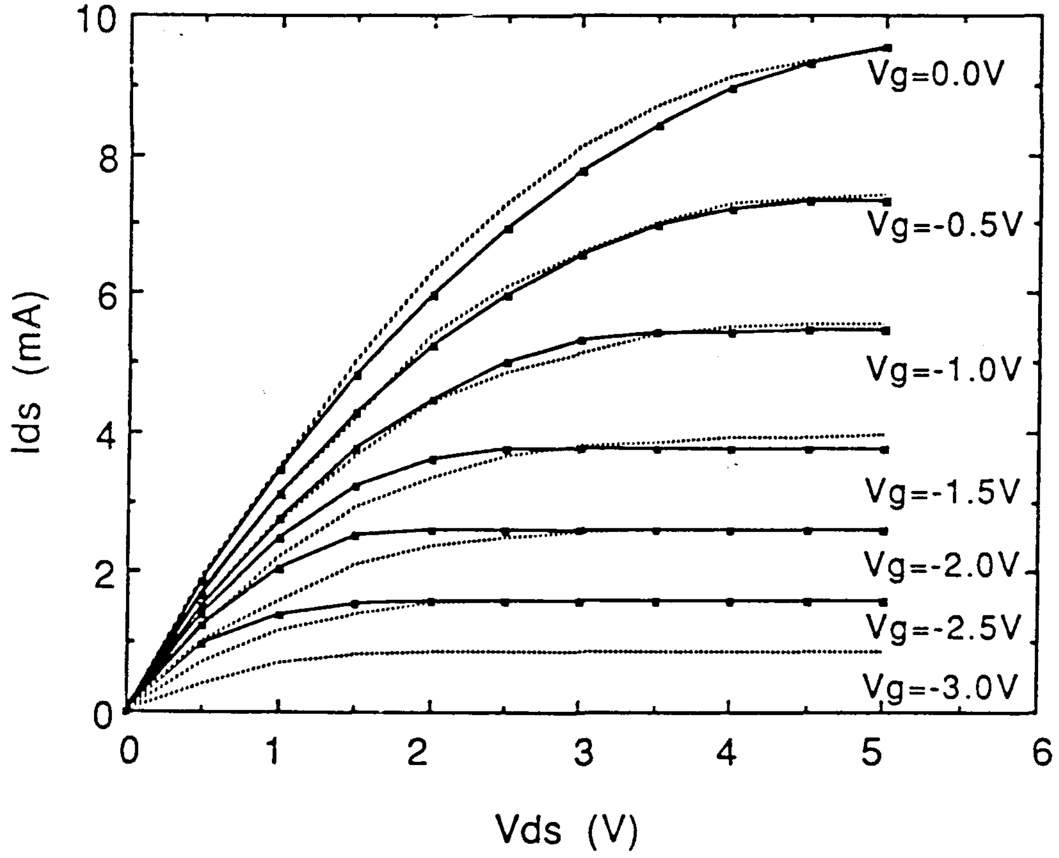

Figure 5.19: Fit of Model B to the measured FATFET I-V characteristics. The solid lines are the fitted curves and the dotted lines are the measured curves.

The same method is applied to the high-low junction carrier profile described earlier. Again an analytical function has been chosen for approximating this curve. Figure 5.20 shows the modelled function with respect to the high-low junction carrier profile. The profile consists of a constant 4×10^{18} cm^{-3} doped region from the interface to 80Å, followed by the region of 80Å<x<2159Å expressed by the function $n = 3.981 \times 10^{23} (x)^{-2.6258}$,and then another constant 7×10^{14} cm^{-3} region from 2159Å to

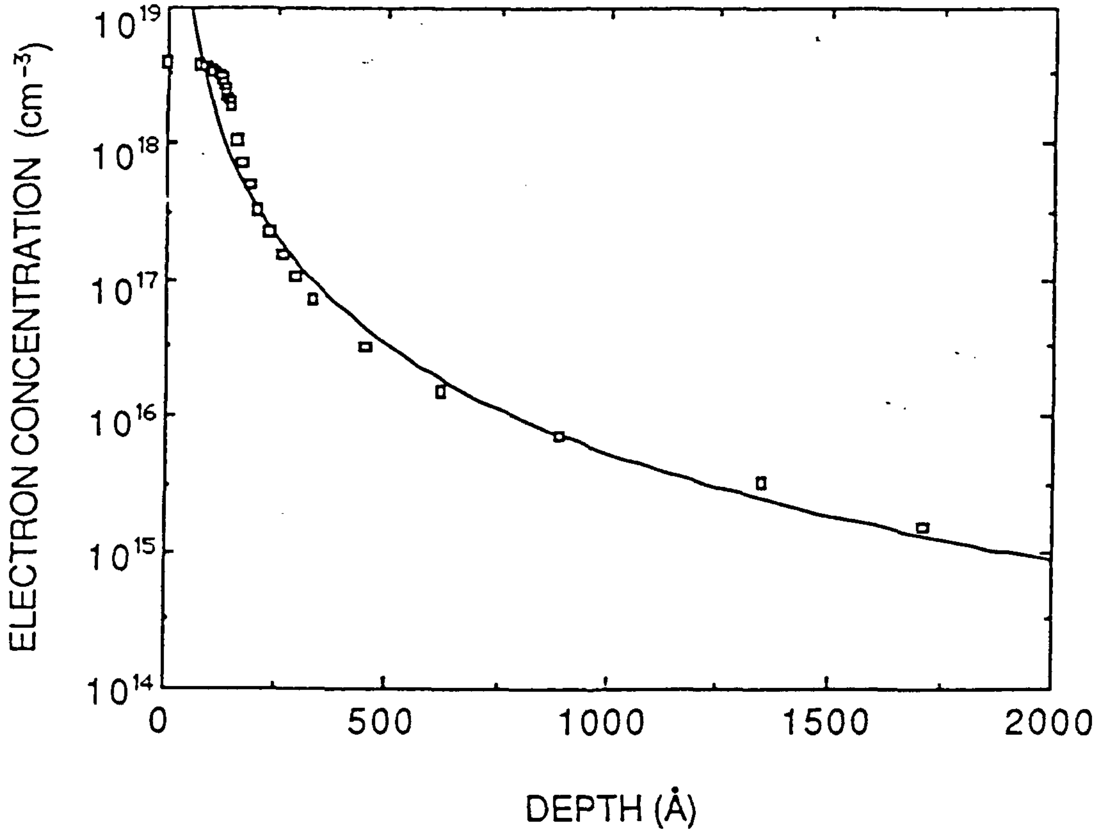

Figure 5.20: Comparison of the analytic function $n = 3.981 \times 10^{23} (x)^{-2.6285}$ shown as the solid line and the profile obtained from the high-low step-junction theoretical calculation.

1μm. The procedure for determining each I-V curve as a function of gate voltage is the same as stated above except that the high-low junction profile replaces the C-V profile when determining the depletion depth and calculating for <n> in the remaining channel. Figure 5.21 illustrates the final fit.

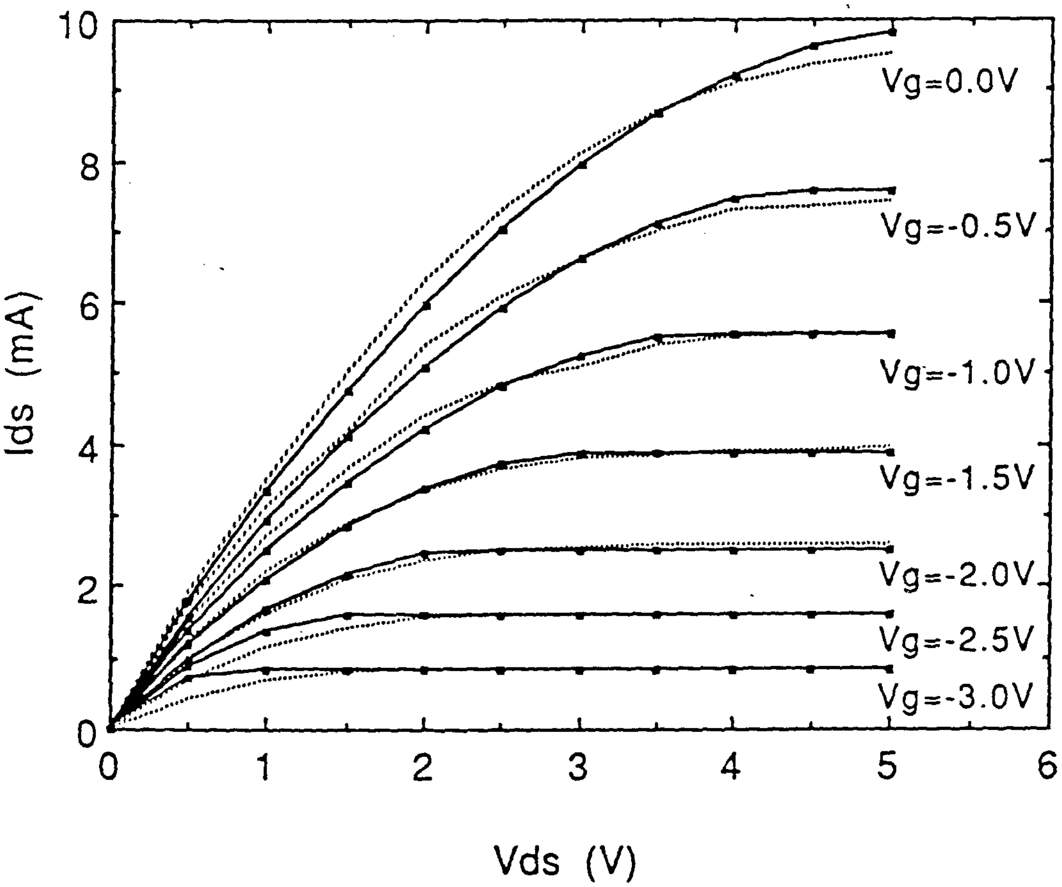

Figure 5.21: Fit of Model C to the measured FATFET I-V characteristics. The solid lines are the fitted curves and the dotted lines are the measured curves.

Conclusions

The operation of a strained-layer InGaAs/InAlAs HIGFET has been demonstrated, with fairly impressive results. The true success, however, is in the spectrum of techniques applied to make this device function. First, the ability to readjust the lattice constant from that of GaAs to that of $In_{0.15}Ga_{0.85}As$. Albeit a small change in lattice constant, it reflects the necessary conditions to relax the structure to a new state, and invites further application to more extreme values. Second, the use of strained layers, in particular strained-layer superlattices, to act as dislocation filters. The successful reduction of dislocations which might otherwise propagate to active regions of the device and degrade device performance allows access to new materials and properties which can now be explored. Next, the HIGFET itself. Undoped depleted InAlAs has been shown to behave as a quasi-insulator. It can be grown lattice matched to the buffer lattice constant and is not affected by the presence of a heavily doped pseudomorphic channel layer directly beneath it. There does not appear to be any degradation in insulator quality although it is an indirect bandgap material. The heavily doped channel may be grown pseudomorphically to extend the material properties and when coupled with the undoped buffer beneath it appears as a high-low junction. From the modelling above, the conduction in the buffer next to the channel must be taken into account. Furthermore, the non-uniform nature of the electron concentration must be considered. The resulting device is reminiscent of ion-implanted MESFETs. However, the intrinsic value of the HIGFET is that the MBE-grown material allows one to grow the implanted region into the device, avoiding damage and annealing steps. The HIGFET itself is only a tool to demonstrate the application of this material system. It suggests that any number of other devices might be attempted, such as the MODFET, SISFET, JFET, or delta-doped HIGFET. And the material does not have to be limited to 30% InAs content but may be extended to channels containing 40% or 50% InAs content, and in general principle to other compounds. The objective is to take advantage of which ever material properties are available and make use of them in whatever type of device that will most benefit.

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